APPLICATION NOTE

(DOC No. HX8238-D -AN)

HX8238-D

960 x 240 TFT LCD Single Chip Digital Driver

version 01 June, 2008

Himax Technologies, Inc.
http://www.himax.com.tw

1. General Description

The HX8238-D application note includes SPI commands, FPC pins, OLB resistance and application circuit. H-Sync (HSYNC), V-Sync (VSYNC), Data enable (DEN), and Clock (DOTCLK) from video decoder or other source. The interface follows digital 8-bit serial/24-bit parallel RGB, CCIR601 and CCIR656 input format.
The HX8238-D is a single chip controller and driver LSI that integrates the power circuit. It can drive a maximum 960x240 dot graphics on a-TFT panel displays in 16.7M colors.

The HX8238-D has a low-voltage operation, 1.4 min. In addition, The HX8238-D is equipped with a DC-DC converter control circuit that generates the supply voltage for source and gate drivers with minimum external components. A common voltage generation circuit is included to drive the TFT-display counter electrode. An integrated gamma control circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

2. SPI Command Setting

2.1 Serial interface

The SPI is available through the chip select line (CSB), serial transfer clock line (SCK), serial data input (SDI), and serial data output (SDO).

The Driver IC recognizes the start of data transfer at the falling edge of CSB input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CSB input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100(Primary SPI Register) or 011101(Secondary SPI Register). Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When the RS = 1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (IB15 to 0---9th ~24th SCK).

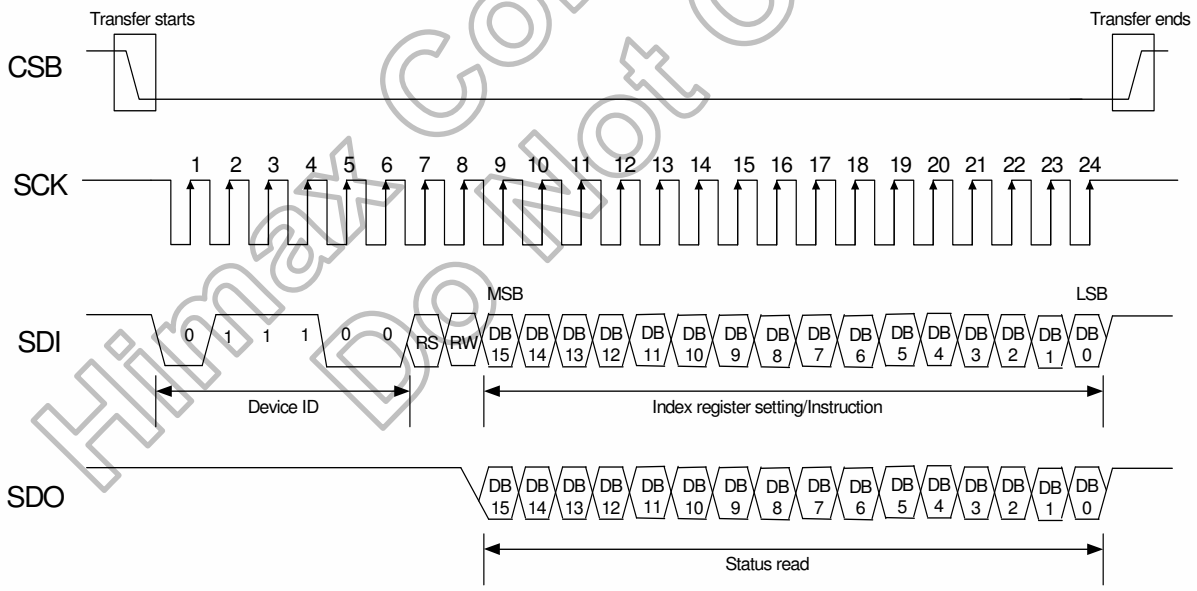


Figure 2. 1 SPI timing

3. Application Circuit

3.1 PWM boost converter

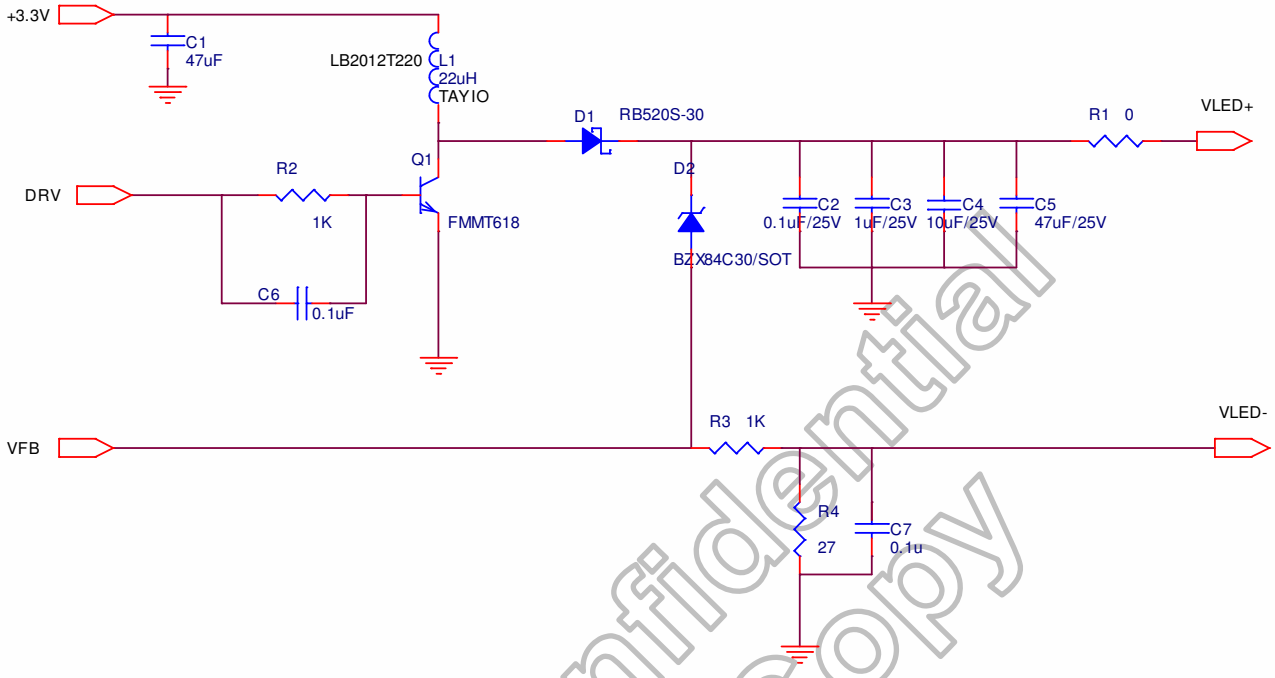


Figure 3. 1 PWM boost converter

3.2 Booster capacitors

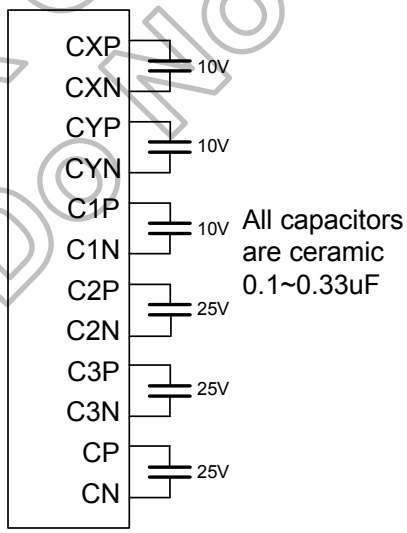


Figure 3. 2 Booster capacitors

3.3 Power supply pins connections

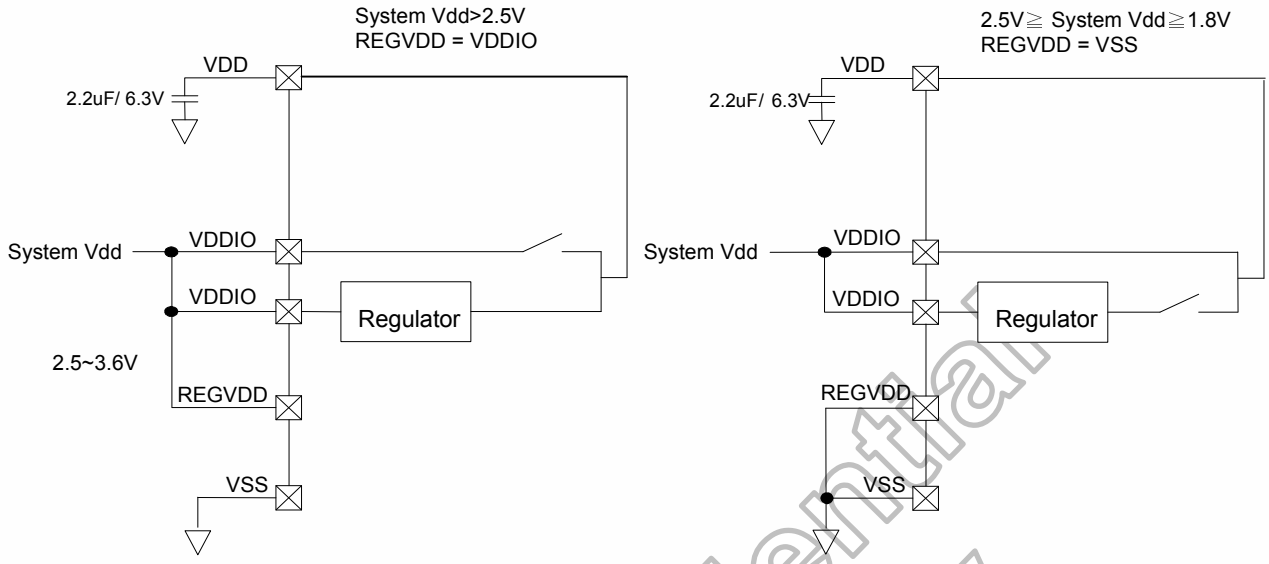
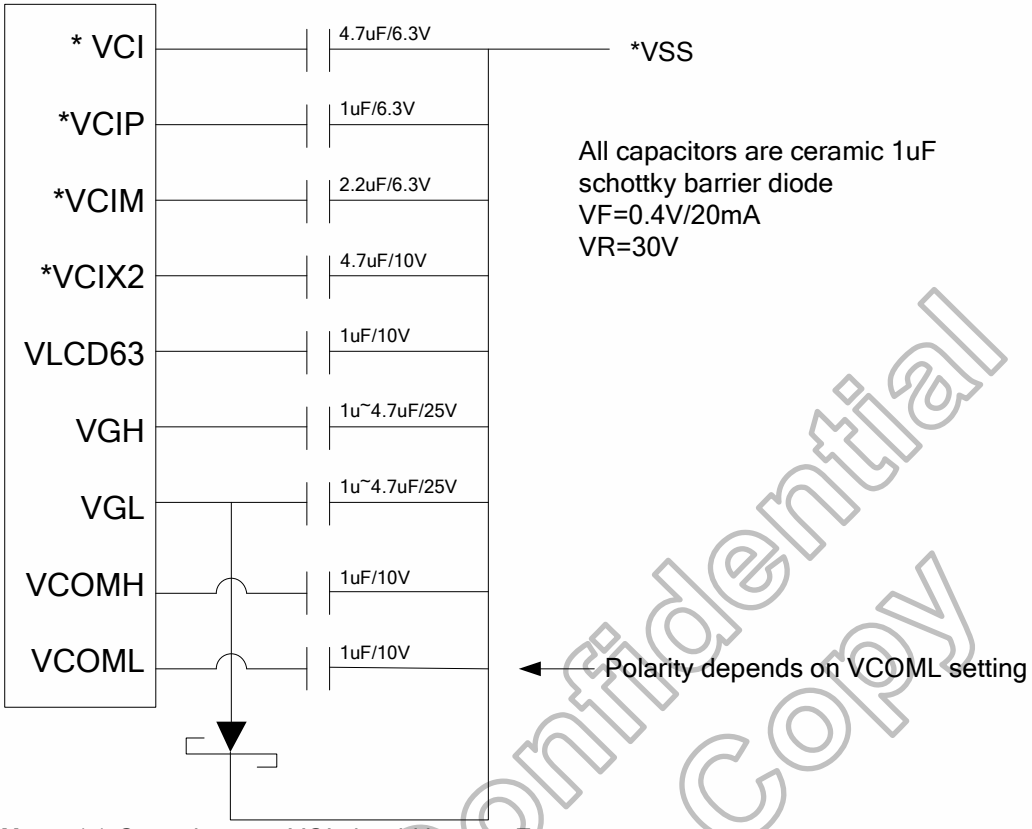


Figure 3. 3 Power supply pins connections

3.4 Filtering and charge sharing capacitors



Note: (1) Capacitors on VCI should be 4.7uF.
(2) Capacitors on VCIM should be 2.2uF
(3) Capacitors on VCIX2 should be 2.2 ~ 4.7uF
(4) Capacitors on VGH, VGL should be 1 ~ 4.7uF
(5) Other capacitors should be 1uF

Figure 3. 4 Filtering and charge sharing capacitors

VCI should be separate with VCIP at ITO layout to provide noise free path
VSS, VCHS, AVSS, and VSSRC should be separated at ITO layout to provide noise free path

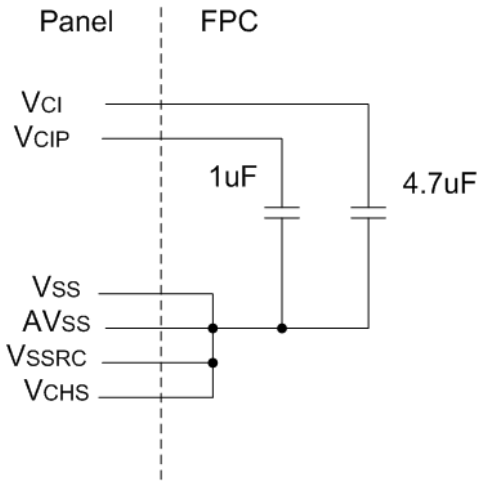


Figure 3. 5 Panel and FPC connection

3.5 Panel connection example

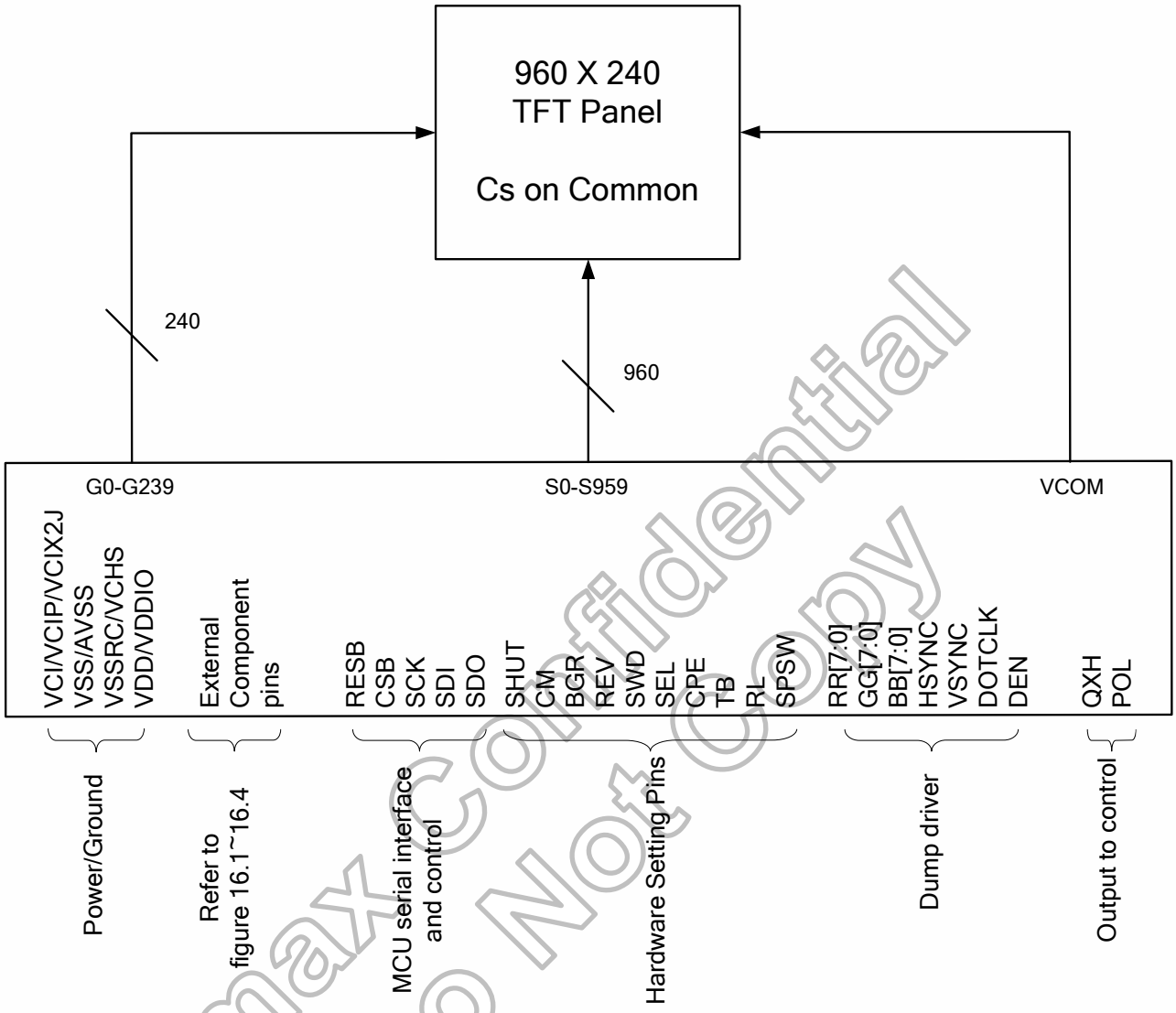


Figure 3. 6 Panel connection example

4. Glass Layout

4.1 Glass layout with internal charge pump (CPE="H") (SPSW="H")

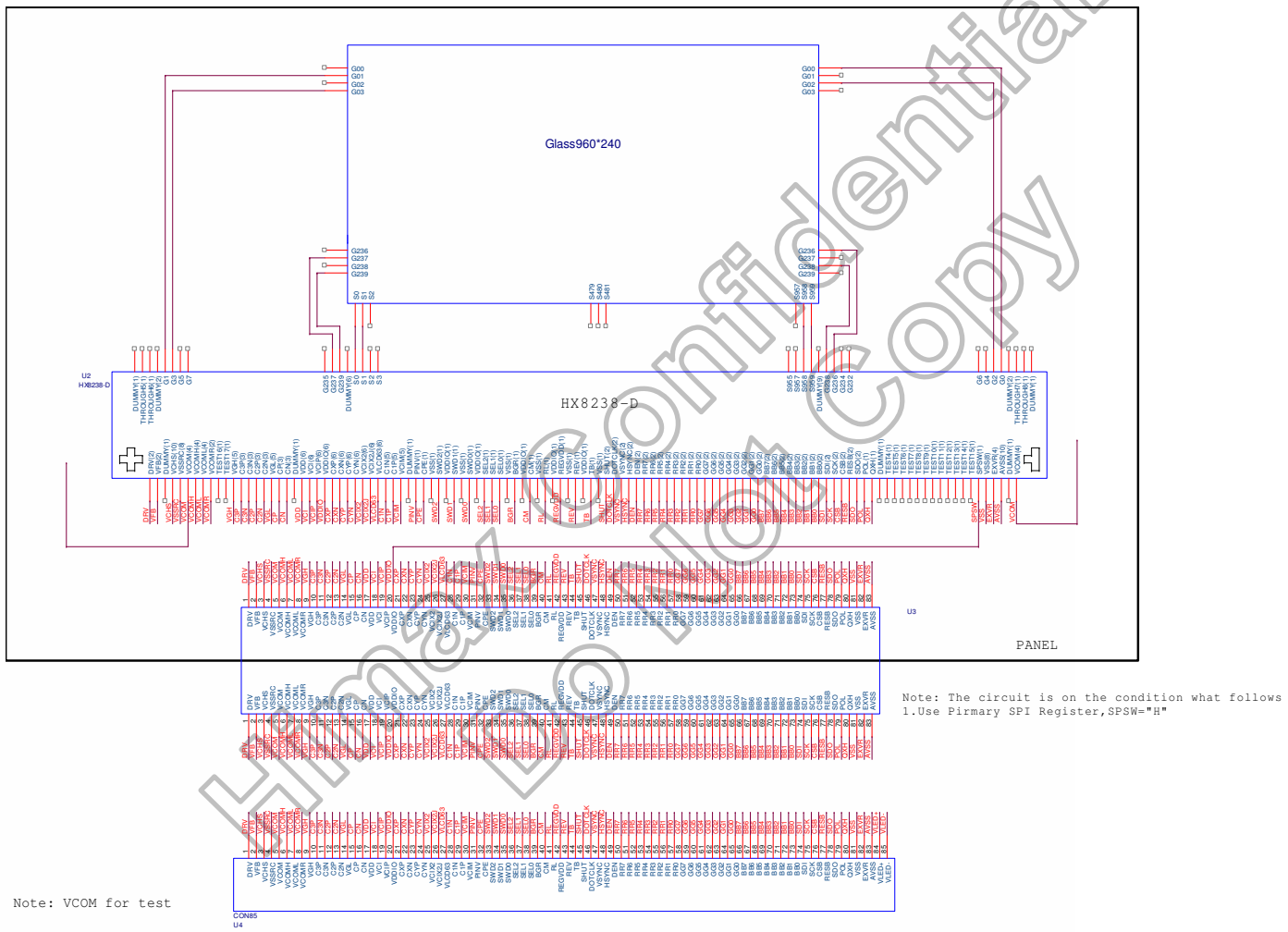
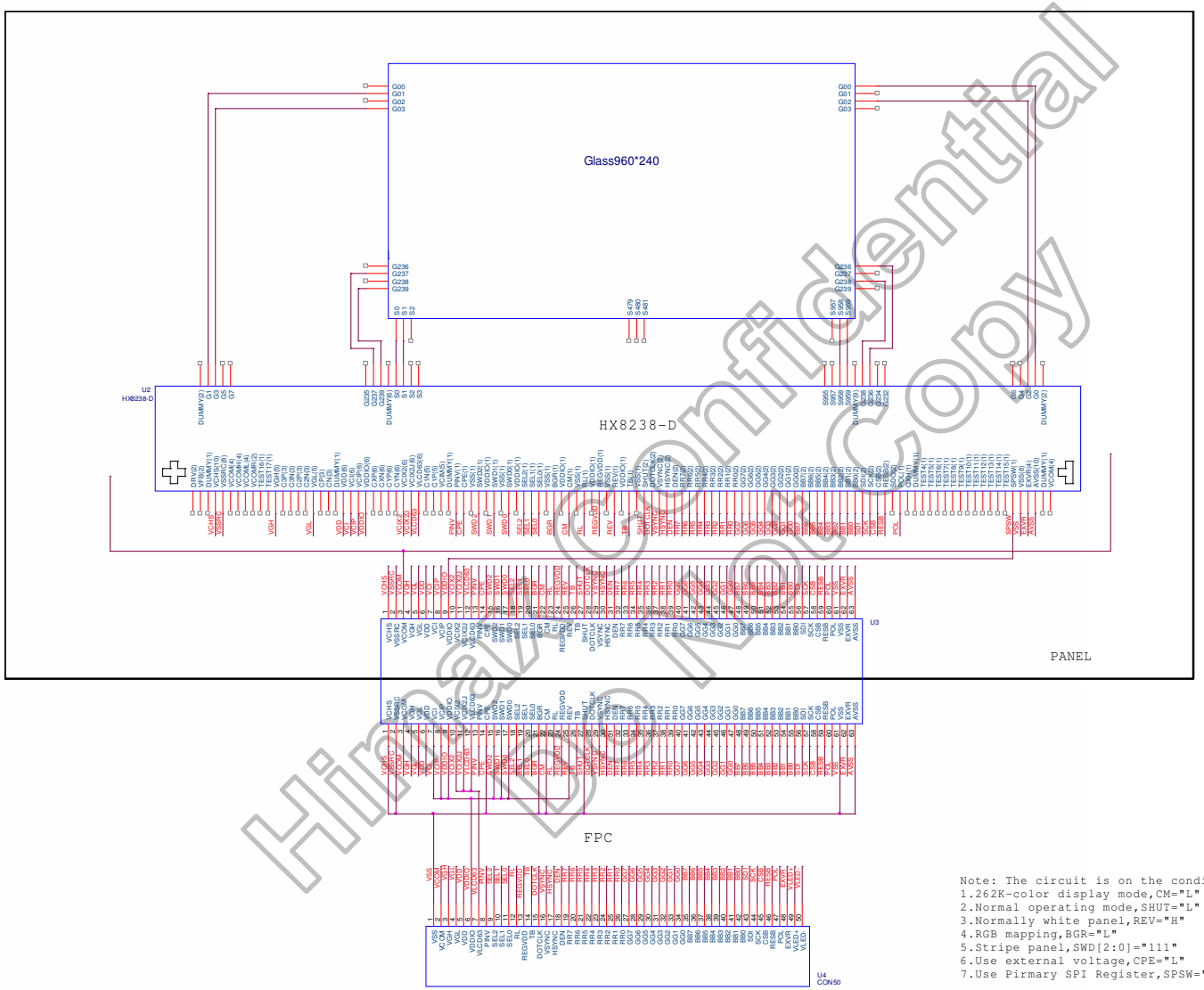


Figure 4. 1 Glass layouts with internal charge pump in primary SPI register

4.2 Glass layout without internal charge pump (CPE="L") (SPSW="H")



Note: The circuit is on the condition what follows
1.262K-color display mode,CM="L"
2.Normal operating mode,SHUT="L"
3.Normally white panel,REV="H"
4.RGB mapping,BGR="L"
5.Stripe panel,SWD[2:0]="111"
6.Use external voltage,CPE="L"
7.Use Pirmary SPI Register,SPSW="H"

Figure 4. 2 Glass layouts without internal charge pump in primary SPI register

4.3 Glass layout without internal charge pump (CPE="H") (SPSW="L")

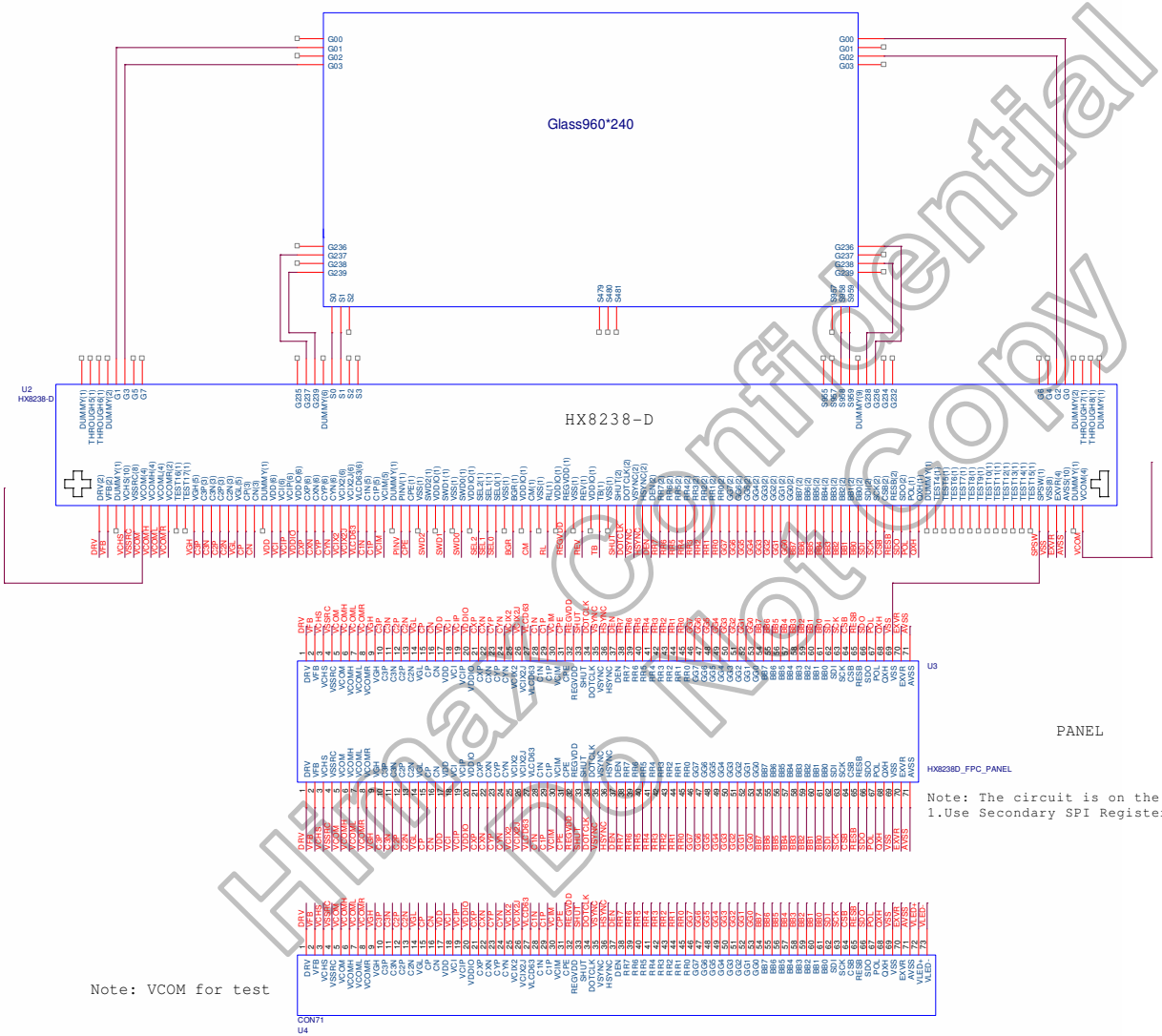


Figure 4. 3 Glass layouts with internal charge pump in secondary SPI register

4.4 Glass layout without internal charge pump (CPE="L") (SPSW="L")

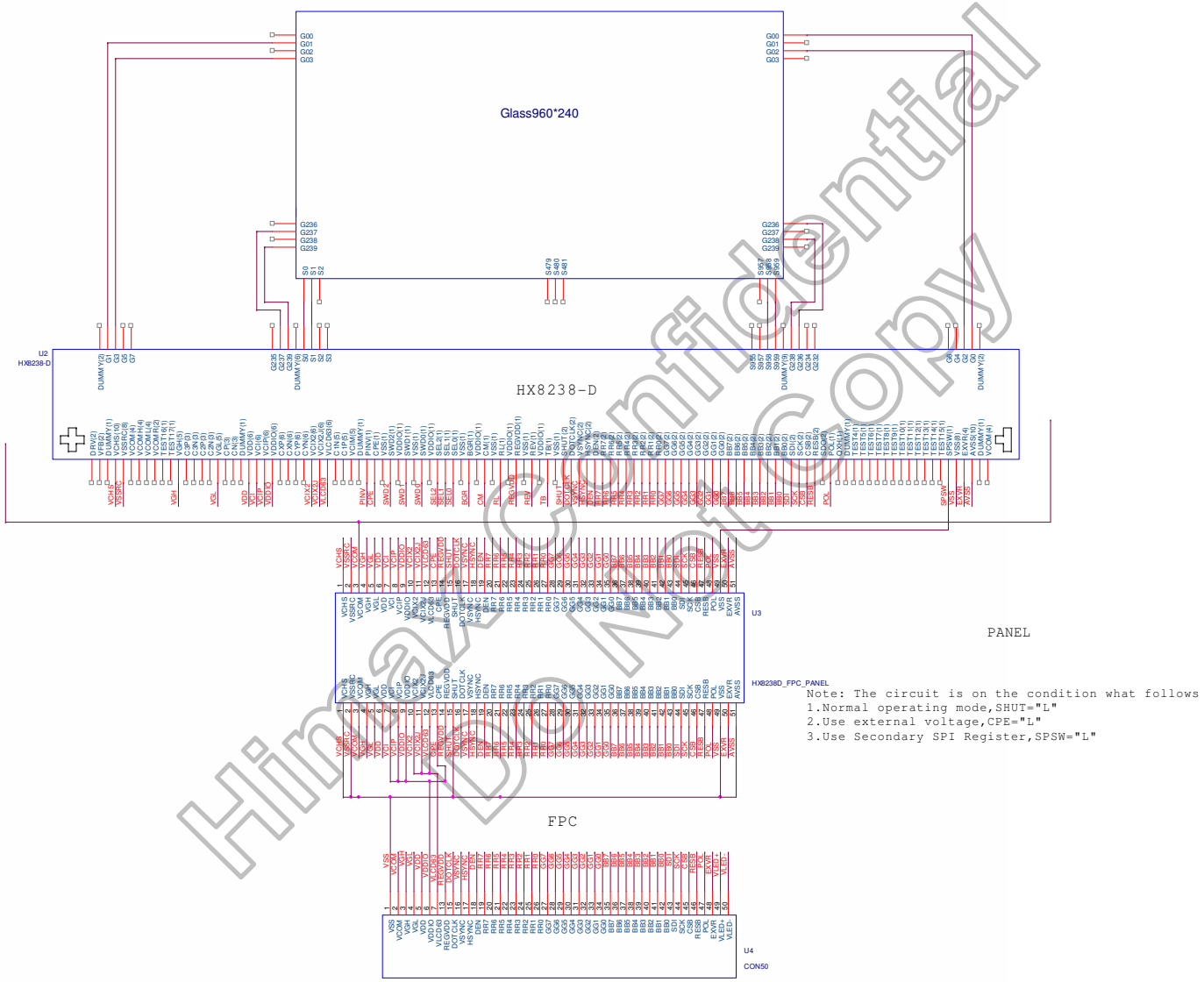


Figure 4. 4 Glass layouts without internal charge pump in secondary SPI register

5. FPC Circuit

5.1 FPC and LED backlight driving circuit with internal charge pump (CPE="H") (SPSW="H")

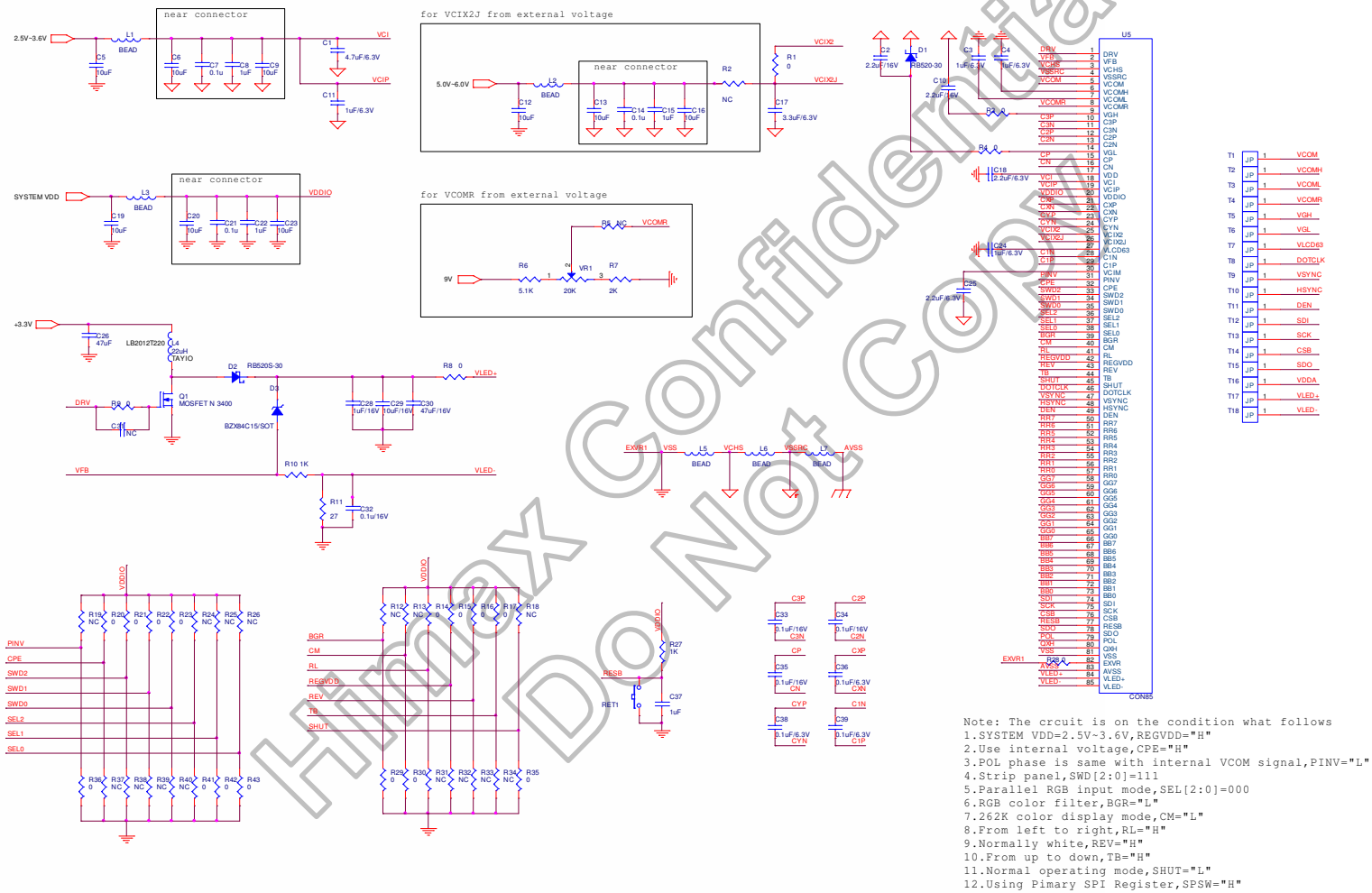


Figure 5. 1 FPC and LED backlight driving circuit with internal charge pump in primary SPI register.

5.2 FPC circuit without charge pump (CPE="L") (SPSW="H")

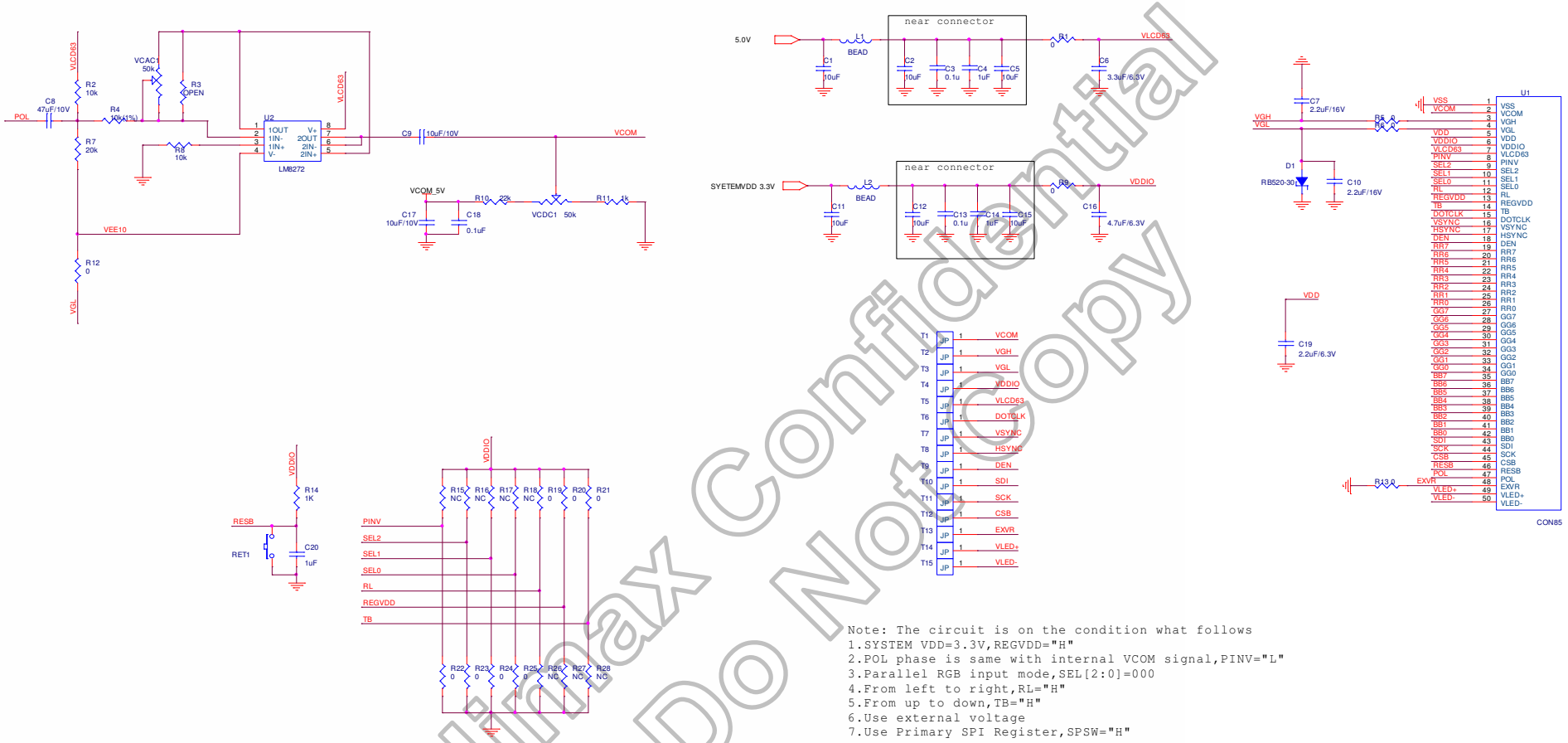


Figure 5. 2 FPC circuit without charge pump in primary SPI register.

5.3 FPC and LED backlight driving circuit with Internal charge pump (CPE="H") (SPSW="L")

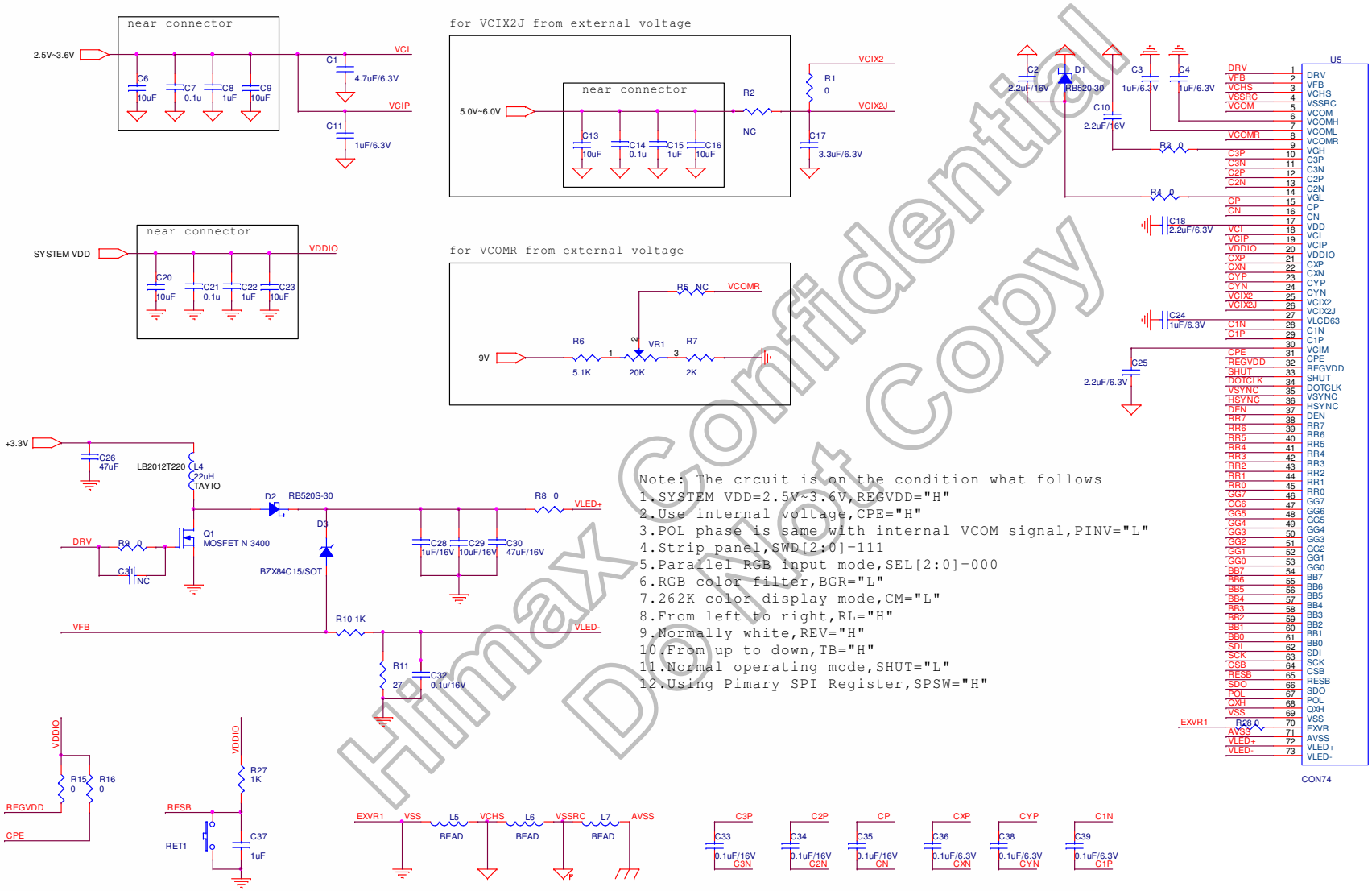


Figure 5. 3 FPC and LED backlight driving circuit with internal charge pump in secondary SPI register.

5.4 FPC circuit without charge pump (CPE="L") (SPSW="L")

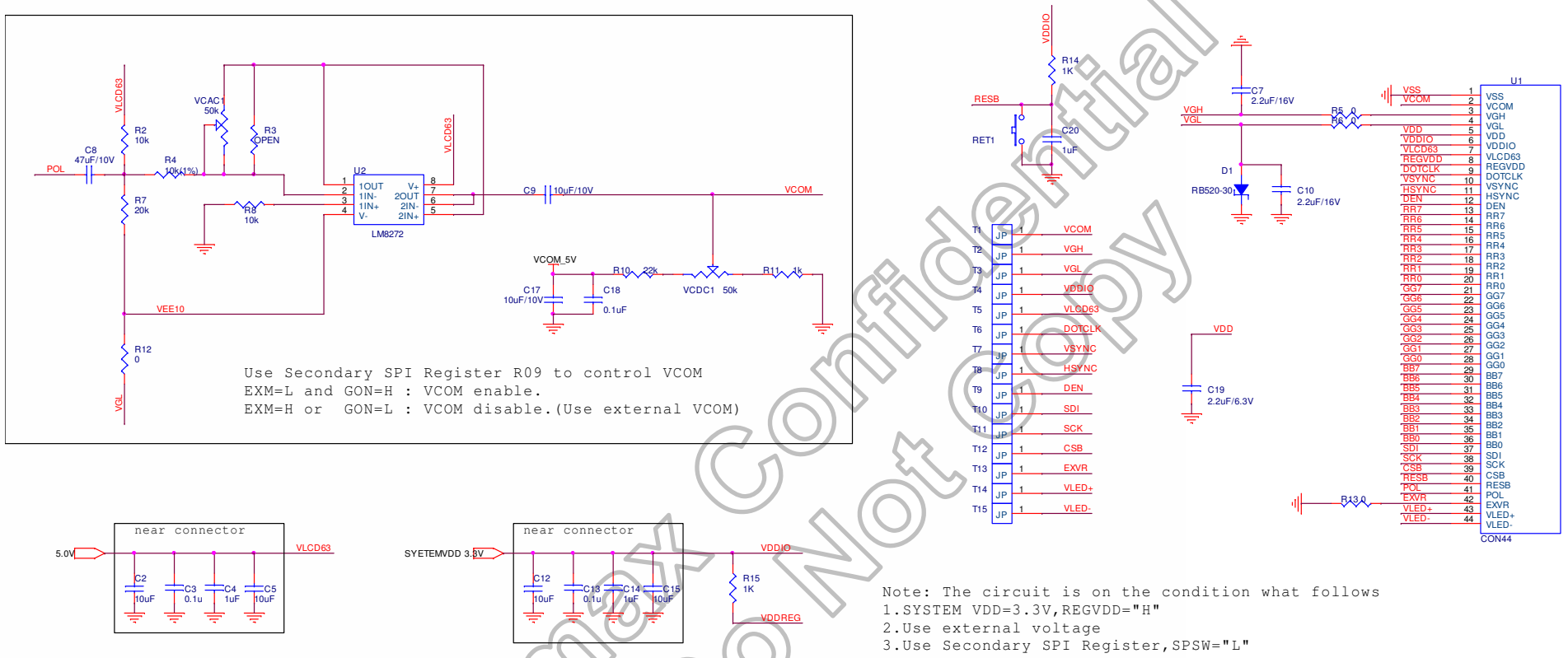


Figure 5. 4 FPC circuit without charge pump in secondary SPI register.

6. OLB Resistance Value

PAD NO.	PAD NAME	Max. Wiring Resistance(Ohm)
1	VCOM	7.5
2	VCOM	
3	VCOM	
4	VCOM	
5	DUMMY	
6	AVSS	5
7	AVSS	
8	AVSS	
9	AVSS	
10	AVSS	
11	AVSS	
12	AVSS	
13	AVSS	
14	AVSS	
15	AVSS	
16	EXVR	7.5
17	EXVR	
18	EXVR	
19	EXVR	
20	VSS	5
21	VSS	
22	VSS	
23	VSS	
24	VSS	
25	VSS	
26	VSS	
27	VSS	
28	DUMMY	
29	TEST15	
30	TEST14	
31	TEST13	
32	TEST12	
33	TEST11	
34	TEST10	
35	TEST9	
36	TEST8	
37	TEST7	
38	TEST6	
39	TEST5	
40	TEST4	
41	DUMMY	
42	QXH	100
43	POL	100
44	SDO	100
45	SDO	100

PAD NO.	PAD NAME	Max. Wiring Resistance(Ohm)
46	RESB	100
47	RESB	
48	CSB	100
49	CSB	
50	SCK	100
51	SCK	
52	SDI	100
53	SDI	
54	BB0	100
55	BB0	
56	BB1	100
57	BB1	
58	BB2	100
59	BB2	
60	BB3	100
61	BB3	
62	BB4	100
63	BB4	
64	BB5	100
65	BB5	
66	BB6	100
67	BB6	
68	BB7	100
69	BB7	
70	GG0	100
71	GG0	
72	GG1	100
73	GG1	
74	GG2	100
75	GG2	
76	GG3	100
77	GG3	
78	GG4	100
79	GG4	
80	GG5	100
81	GG5	
82	GG6	100
83	GG6	
84	GG7	100
85	GG7	
86	RR0	100
87	RR0	
88	RR1	100
89	RR1	

PAD NO.	PAD NAME	Max. Wiring Resistance(Ohm)
90	RR2	100
91	RR2	
92	RR3	100
93	RR3	
94	RR4	100
95	RR4	
96	RR5	100
97	RR5	
98	RR6	100
99	RR6	
100	RR7	100
101	RR7	
102	DEN	100
103	DEN	
104	HSYNC	100
105	HSYNC	
106	VSYNC	100
107	VSYNC	
108	DOTCLK	100
109	DOTCLK	
110	SHUT	100
111	SHUT	
112	VSS	
113	TB	100
114	VDDIO	
115	REV	100
116	VSS	
117	REGVDD	100
118	VDDIO	
119	RL	100
120	VSS	
121	CM	100
122	VDDIO	
123	BGR	100
124	VSS	
125	SEL0	100
126	SEL1	100
127	SEL2	100
128	VDDIO	
129	SWD0	100
130	VSS	
131	SWD1	100
132	VDDIO	
133	SWD2	100
134	VSS	
135	CPE	100
136	PINV	100

PAD NO.	PAD NAME	Max. Wiring Resistance(Ohm)
137	DUMMY	
138	VCIM	10
139	VCIM	
140	VCIM	
141	VCIM	
142	VCIM	
143	C1P	10
144	C1P	
145	C1P	
146	C1P	
147	C1P	
148	C1N	10
149	C1N	
150	C1N	
151	C1N	
152	C1N	
153	VLCD63	10
154	VLCD63	
155	VLCD63	
156	VLCD63	
157	VLCD63	
158	VLCD63	
159	VCIX2J	5
160	VCIX2J	
161	VCIX2J	
162	VCIX2J	
163	VCIX2J	
164	VCIX2J	
165	VCIX2	5
166	VCIX2	
167	VCIX2	
168	VCIX2	
169	VCIX2	
170	VCIX2	
171	CYN	5
172	CYN	
173	CYN	
174	CYN	
175	CYN	
176	CYN	
177	CYP	5
178	CYP	
179	CYP	
180	CYP	
181	CYP	
182	CYP	

PAD NO.	PAD NAME	Max. Wiring Resistance(Ohm)
183	CXN	5
184	CXN	
185	CXN	
186	CXN	
187	CXN	
188	CXN	
189	CXP	5
190	CXP	
191	CXP	
192	CXP	
193	CXP	
194	CXP	
195	VDDIO	10
196	VDDIO	
197	VDDIO	
198	VDDIO	
199	VDDIO	
200	VDDIO	
201	VCIP	10
202	VCIP	
203	VCIP	
204	VCIP	
205	VCI	5
206	VCI	
207	VCI	
208	VCI	
209	VCI	
210	VCI	
211	VCI	
212	VCI	
213	VCI	
214	VCI	
215	VDD	7.5
216	VDD	
217	VDD	
218	VDD	
219	VDD	
220	VDD	
221	DUMMY	
222	CN	10
223	CN	
224	CN	
225	CP	10
226	CP	
227	CP	

PAD NO.	PAD NAME	Max. Wiring Resistance(Ohm)
228	VGL	10
229	VGL	
230	VGL	
231	VGL	
232	VGL	
233	C2N	10
234	C2N	
235	C2N	
236	C2P	10
237	C2P	
238	C2P	
239	C3N	10
240	C3N	
241	C3N	
242	C3P	10
243	C3P	
244	C3P	
245	VGH	10
246	VGH	
247	VGH	
248	VGH	
249	VGH	
250	TEST17	
251	TEST16	
252	VCOMR	100
253	VCOMR	
254	VCOML	7.5
255	VCOML	
256	VCOML	
257	VCOML	
258	VCOMH	7.5
259	VCOMH	
260	VCOMH	
261	VCOMH	
262	VCOM	7.5
263	VCOM	
264	VCOM	
265	VCOM	
266	VSSRC	7.5
267	VSSRC	
268	VSSRC	
269	VSSRC	
270	VSSRC	
271	VSSRC	
272	VSSRC	
273	VSSRC	

PAD NO.	PAD NAME	Max. Wiring Resistance(Ohm)
274	VCHS	5
275	VCHS	
276	VCHS	
277	VCHS	
278	VCHS	
279	VCHS	
280	VCHS	
281	VCHS	
282	VCHS	
283	VCHS	
284	DUMMY	
285	VFB	50
286	VFB	
287	DRV	100
288	DRV	

Note: VFB should not be coupled by other signals in order to provide noise free path.

Table 6. 1 OLB resistance value

7. Power On/Off Sequence

Power on sequence	
1	VDDIO power on
2	wait > 1ns
3	VCI/VDD power on
4	wait > 10us
5	RESB go High
6	Input control timing (DOTCLK/HSYNC/VSYNC/…)
7	Select input data interface by SEL[2:0] of R04h if necessary
8	Set VBP[6:0]/HBP[6:0] (R17h) to meet input data timing
9	Set gamma voltage by R30h~R37h
10	Set "nOTP" bit in R1Eh to "1" to make VCOM controlled by register
11	Set VCOMH voltage by VCM[6:0] of R1Eh
12	Set VCOM amplitude by VDV[6:0] of R0Eh
13	Set PWM to turn on in R05h if necessary
14	wait > 1us
15	SHUT go Low
16	LCD display will be normal after 14 frames

Power off sequence	
1	SHUT go High
2	wait > 10us
3	Set PWM to turn off in R05h if necessary
4	Wait > 2 frames
5	Stop input signals
6	VCI/VDD power off
7	VDDIO power off

7.1 Power up/down sequence of the secondary register command

When set to Secondary Register command and CPE=VSS, the charge pump circuit will not enable and the VCIX2, VGH, VGL need to external input.

VCOM can be selected to internal generation or external input by setting register R09h EXM or GON, it needs set both EXM=0 and GON=1, VCOM will be internal generated. If each EXM=1 or GON=0, then VCOM circuit will be disabled, and VCOM need to be external input.

Please follow the recommend power up/down sequence as below steps:
(Set VCOM is external inputted.)

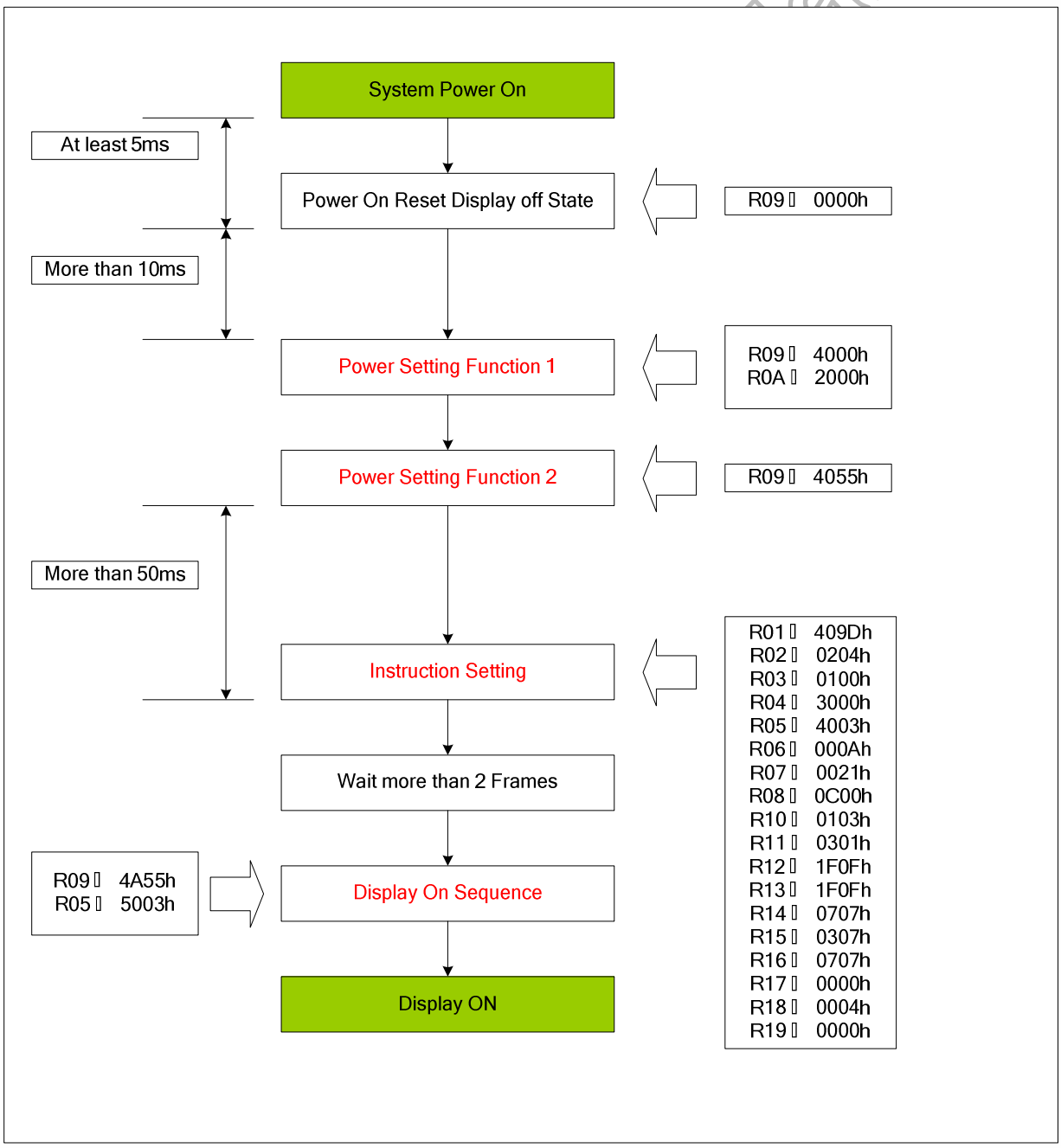


Figure 7. 1 Power up sequence when SPSW connect to VSS (CPE = VSS)

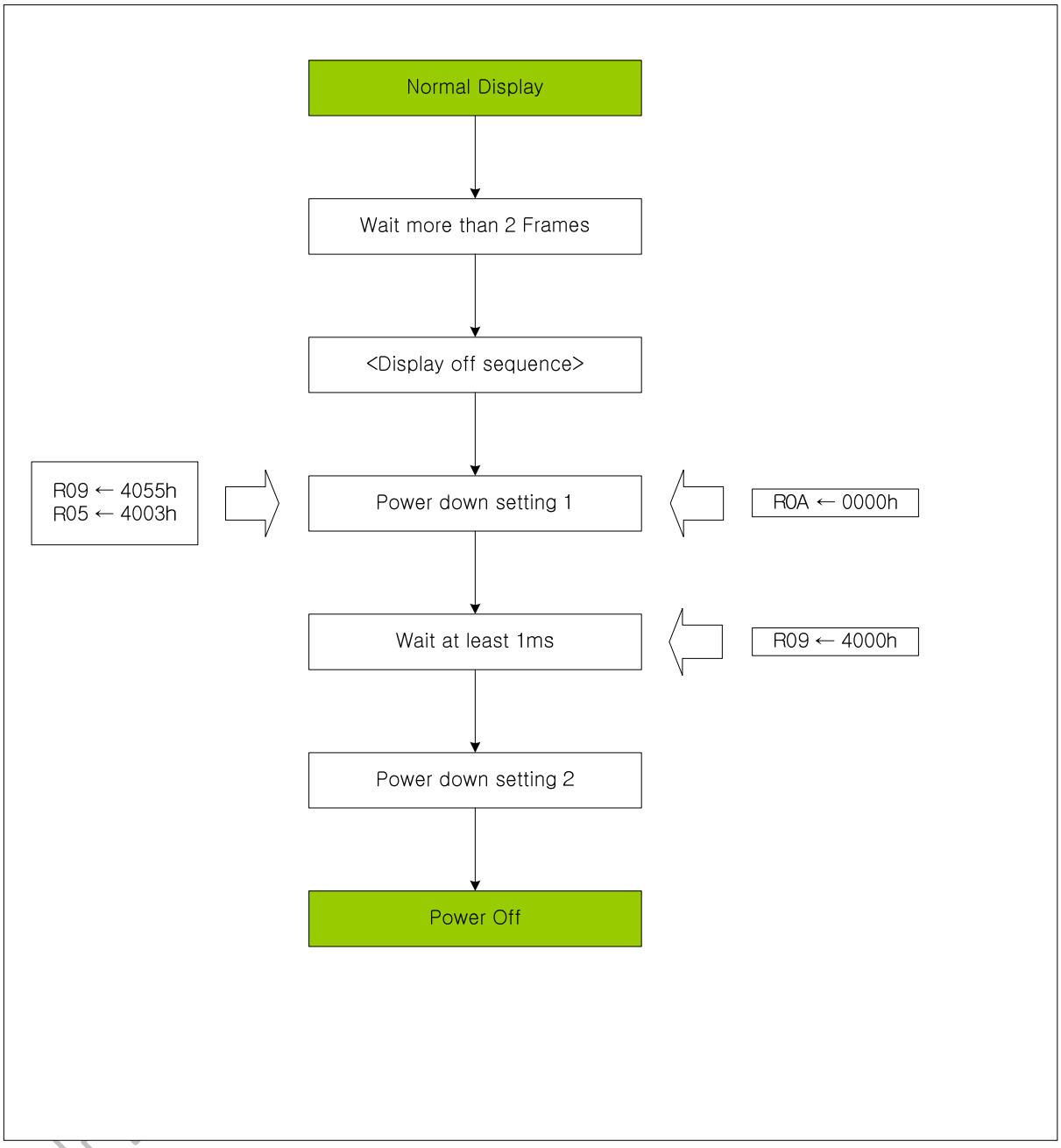


Figure 7. 2 Power down sequence when SPSW connect to VSS (CPE = VSS)

When set to Secondary register command and CPE=VDDIO, the charge pump circuit will enable and the VCIX2, VGH, VGL, VCOM will internal generation.

8. OTP Programming

OTP write sequence

Step	Operation
1	Power up the module. Set nOTP=1 and find out the appropriate value of VCM[6:0] and power off the system
2	Power up the system with VDD=VDDIO=2.5V. If REGVDD=1, set R0Dh=16'h0324.
3	Set appropriate values found from step 1 to register of VCOM (R1Eh)
4	Set R06h=16'h2820 to stop VGH/VGL pumping. Wait 0.5s.
5	Set R60h=16'h8000
6	Set R60h=16'hC000
7	Connect 7.3V to VGH and 0V to VGL (Note1)
8	Set R60h=16'hC200
9	Set R60h=16'hC280
10	Wait 200us for completing this program
11	Set R60h=16'hC200
12	Remove 7.3V from VGH and 0V from VGL
13	Set R60h=16'h8200
14	Set R60h=16'h0200
15	Set R60h=16'h0040
16	Set R60h=16'h0000

Note: VGH is connected to 7.1~7.4

Table 8. 1 OTP programming sequence

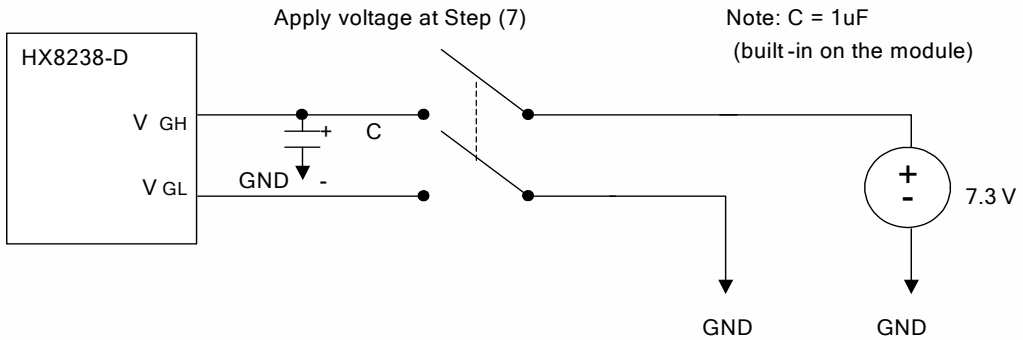
You can use above programming sequence to set VCM [6:0] value to OTP cell once. Before you program the OTP cell, the default VCM [6:0] =1011111 in OTP of Part NO. If you want to check if the OTP cell is till available for programming, you can read the status from R61h shown below.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	IND[2]	VCM6[2]	VCM5[2]	VCM4[2]	VCM3[2]	VCM2[2]	VCM1[2]	VCM0[2]	IND[1]	VCM6[1]	VCM5[1]	VCM4[1]	VCM3[1]	VCM2[1]	VCM1[1]	VCM0[1]

Table 8. 2 OTP read table

You can check the IND[2] bit to see if the VCM[6:0] is still programmable or not. If IND[2]=0, you can program new VCM[6:0] value to OTP. If IND[2]=1, it means that the OTP cell have already programmed twice and you can't program it any more. IB6~IB0 indicate the currently effective VCM[6:0] setting in OTP cell.

OTP Programming circuitry



Note: The pad of VGH and VGL must be retained on the system board to offer the voltage for OTP programming

Figure 8. 1 OTP programming circuitry

9. Revision History

Version	Date	Description of Changes
01	2008/03/05	New setup