SPECIFICATION

MODULE NO.: YH070BS31-MI01

REVISION 00

Customer Approval:

	SIGNATURE	DATE
PREPARED BY (RD ENGINEER)	HDW	July -11-2023
PREPARED BY (QA ENGINEER)	PJ	July -11-2023
CHECKED BY	LBQ	July -11-2023
APPROVED BY	CYM	July -11-2023

DOCUMENT REVISION HISTORY

Version	DATE	DESCRIPTION	CHANGED BY
00	DECE-13-2023	First Issue	HDW

1.0 General Description

1.1 Introduction

YH070BS31-MI01 Display model 7.0” LCM is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel and a driving circuit.This TFT LCD has a 7.0(16:9) inch diagonally measured active display area with (1024horizontal by 600 vertical pixel) resolution.

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	
Screen Size	7.0	Inch	Diagonal
Resolution	1024(W)*3(RGB)*600(H)	Dots	
Interface	MIPI	-	4lane
Module Power Consumption	1.433	Watt	Typ.
Active Area	154.21(W)*85.92(H)	mm	
Pixel pitch (W*H)	0.143(W)*0.0502(H)	mm	
Module Size (W*H*D)	164.8(W)*100(H)*3.5(D)	mm	Tolerance:±0.2
Luminance	400	cd/m^2	Typ.
Viewing Direction	All	O’clock	-
Display Color	16.7M	Colors	24bits

2.0 ABSOLUTE MAXIMUM RATINGS

The following are maximum values which, if exceeded may cause operation or damage to the unit.

Item	Symbol	Min	Max	Unit	Note
Digital Supply Voltage	VDD	-0.3	3.96	V	
Analog Supply Voltage	AVDD	-0.5	14.85	V	
Gate On Voltage	VGH	-0.3	40	V	
Gate Off Voltage	VGL	-20	0.3	V	

Note :If users use the product out off the environment operation range (temperature and humidity ,it will have visual quality concerns

3.0 ELECTRICAL CHARACTERISTICS

3.1 Typical Operation Condition

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage	VDD	3.0	3.3	3.6	V	-
Analog Power Supply Voltage	AVDD	10	11	11.9	V	-
Gate On Power Supply Voltage	VGH	19	20	21	V	-
Gate Off Power Supply Voltage	VGL	-8	-7	-6	V	-
Common Power Supply Voltage	VCOM	3.2	3.6	3.9	V	-

TFT-LCD Current Consumption

Item	Symbol	Condition	Min.	TYP	Max.	Unit	NOTE
Gate on Current	IVGH	VGH=18		0.31		MA	
Gate off Current	IVGL	VGL=-6.0		0.45		MA	
Digital Current	IVDD	VDD=3.3		21		MA	
Analog Current	IAVDD	AVDD=9.6		30		MA	
LED Current	ILED			20		MA	

3.2 BACKLIGHT CHARACTERISTICS

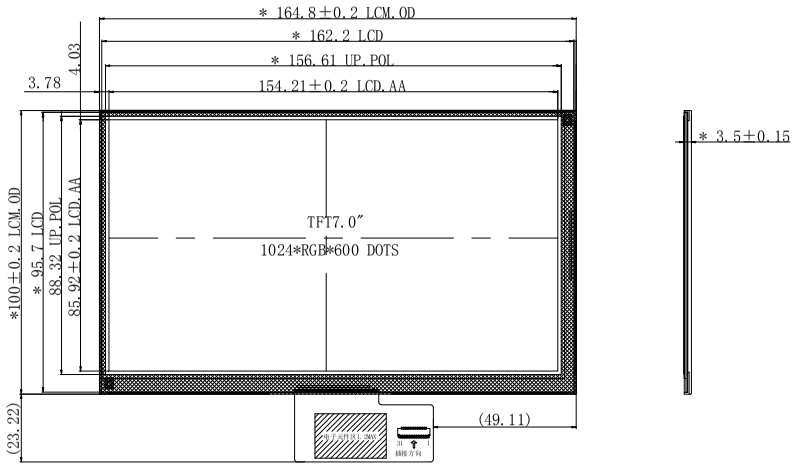
Item	Symbol	Min	Typ	Max	Unit	Condition
Forward voltage	Vf	9.0	9.6	10.5	V	If=180mA
Luminance	Lv	350	400		cd/m2	If=180mA
Number of LED	--	27			Piece	--
Connection mode	P	3chips serial *9			--	--

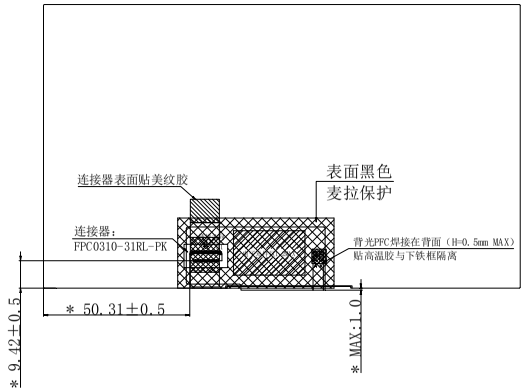
3. MECHANICAL DRAWING

REV.	CONTENT	DESIGN	DATE
A	FIRST REALEASE	肖喜亮	
B			

PIN	SYMBOL
1	LED+
2	LED+
3	LED+
4	NC
5	LED-
6	LED-
7	LED-
8	LED-
9	GND
10	GND
11	MIPI_2P
12	MIPI_2N
13	GND
14	MIPI_1P
15	MIPI_1N
16	GND
17	MIPI_CLKP
18	MIPI_CLKN
19	GND
20	MIPI_0P
21	MIPI_0N
22	GND
23	MIPI_3P
24	MIPI_3P
25	GND
26	VDDIO
27	RESET
28	GND
29	VDDIO
30	VDD
31	VDD

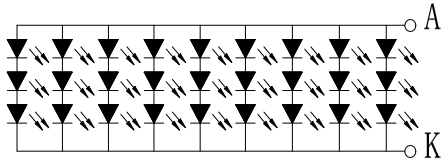
正视图　　侧视图　　背视图





FPC弯折示意图

FPC弯折出货



LED CIRCUIT DIAGRAM

Vf=8.4-10.2V(If=180mA)

NOTES:

1. DISPLAY TYPE:7.0" 1024*600 TFT LCD
   TRANSMISSVE NORMALLY BLACK
2. VIEWING ANGLE(L/R/U/D):85/85/85/85
3. OPERATING TEMPERATURE:0° C TO 50° C;
   STORAGE TEMPERATURE:-10° C TO 60° C,

MODUEL NO.		DRAWN		
TITLE	LCM	CHECKED		UNIT MM
SCALE 1:1	第三视角	APPROVE		PAGE 1/1

4.0 Interface Pin Connection

TFT LCD Module

PIN NO	SYMBOL	DESCRIPTION
1	LEDA	Power for LED backlight (Anode)
2	LEDA	Power for LED backlight (Anode)
3	LEDA	Power for LED backlight (Anode)
4	NC	No connect.
5	LEDK	Power for LED backlight (Cathode)
6	LEDK	Power for LED backlight (Cathode)
7	LEDK	Power for LED backlight (Cathode)
8	LEDK	Power for LED backlight (Cathode)
9	GND	Ground
10	GND	Ground
11	MIPI_D2+	HSSI_D2_Pare differential small amplitude signals.
12	MIPI_D2-	HSSI_D2_Nare differential small amplitude signals.
13	GND	Ground
14	MIPI_D1+	HSSI_D1_Pare differential small amplitude signals.
15	MIPI_D1-	HSSI_D1_Nare differential small amplitude signals.
16	GND	Ground.
17	MIPI_CLK+	HSSI_CLK_P are differential small amplitude signals
18	MIPI_CLK-	HSSI_CLK_N are differential small amplitude signals
19	GND	Ground.
20	MIPI_D0+	HSSI_D0_P are differential small amplitude signals.
21	MIPI_D0-	HSSI_D0_N are differential small amplitude signals.
22	GND	Ground.
23	MIPI_D3+	HSSI_D3_P are differential small amplitude signals.
24	MIPI_D3-	HSSI_D3_N are differential small amplitude signals.
25	GND	Ground.
26	TE	Output for monitoring
27	RESET	Global reset pin.
28	ID	Ground. If no used, Please No Connect.
29	IOVCC	Power supper 1.8V
30	VCI	Power supper 3.0-3.6 V
31	VCI	Power supper 3.0-3.6 V

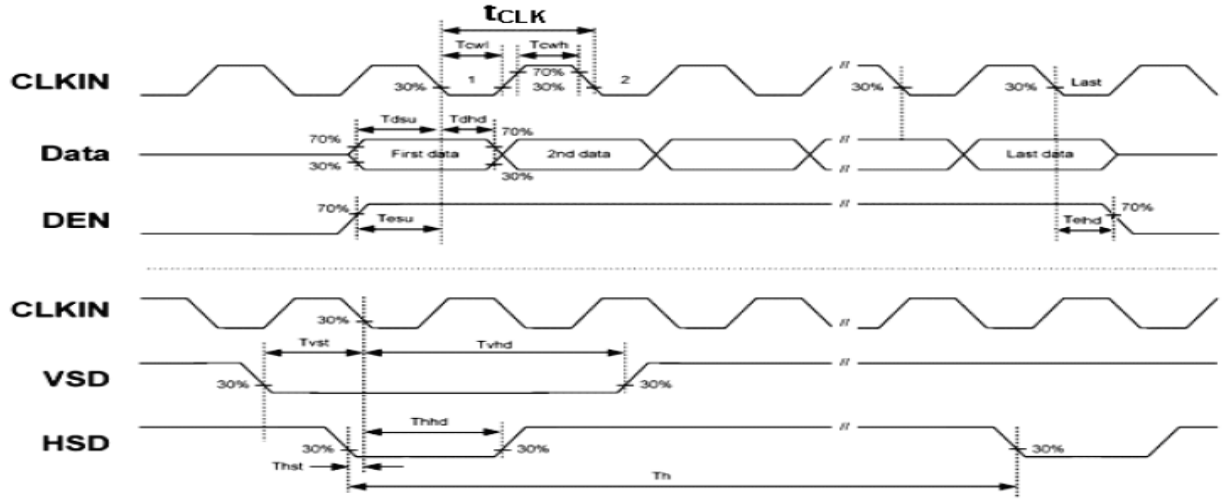
5.0 TIMING CHARACTERISTICS OF INPUT SIGNAL

5.1 Input Timing Table

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	Note
DE MODE	Dot Clock	1/tCLK	45	51.2	57	MHz	
	DCLK Pulse Duty	Tcwh	40	50	60	%	
	Horizontal Total Time	tH	1324	1344	1364	tCLK	
	Horizontal Effective Time	tHA		1024		tCLK	
	Horizontal Blank Time	tHB	300	320	340	tCLK	
	Vertical Total Time	tV	625	635	645	tH	
	Vertical Effective Time	tVA		600		tH	
	Vertical Blank Time	tVB	25	35	45	tH	
SYNC MODE	Horizontal Total Time	TH	1324	1344	1364	tCLK	
	Horizontal Pulse Width	Thpw		20	-	tCLK	thb + thpw =160DCLK is fixed
	Horizontal Back Porch	Thb		140	-	tCLK	
	Horizontal Front Porch	Thfp	140	160	180	tCLK	
	Horizontal Effective Time	THA		1024		tCLK	
	Vertical Total Time	TV	625	635	645	tH	
	Vertical Pulse Width	Tvpw		3	-	th	tvpw + tvb =23th is fixed
	Vertical Back Porch	Tvb	-	20	-	th	
	Vertical Front Porch	Tvfp	2	12	22	th	
	Vertical Valid	Tvd		600		th	

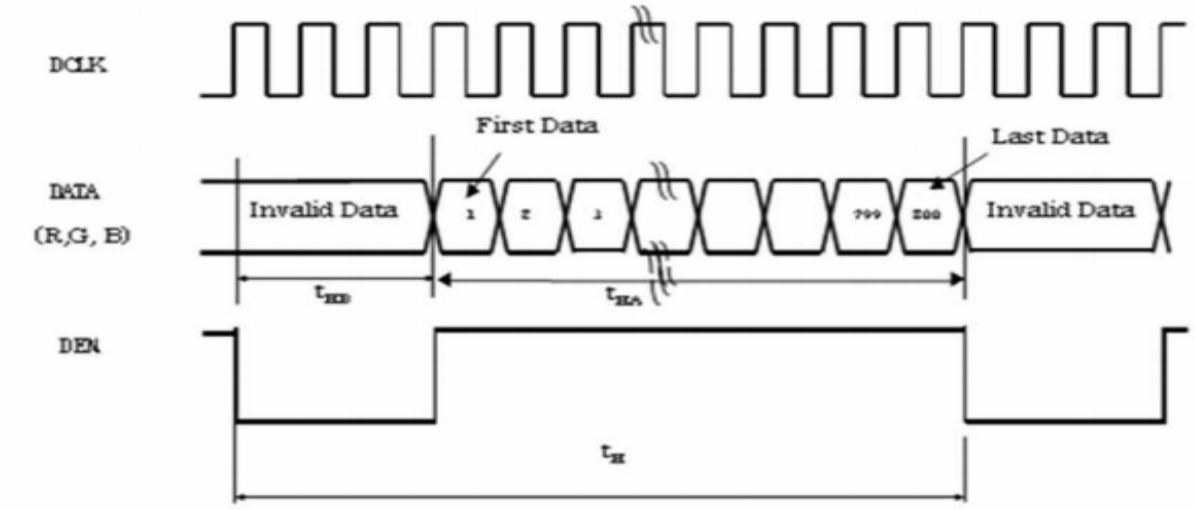
5.2 Input Clock and Data Timing Diagram

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
DVDD Power On Slew Rate	TPOR	-	-	20	ms	From 0V to 90% DVDD
RSTB Pulse Width	TRst	50	-	-	us	DCLK=65MHz
DCLK Cycle Time	Tcph	14	-	-	ns	
DCLK Pulse Duty	Tcwh	40	50	60	%	
VSD Setup Time	Tvst	5	-	-	ns	
VSD Hold Time	Tvhd	5	-	-	ns	
HSD Setup Time	Thst	5	-	-	ns	
HSD Hold Time	Thhd	5	-	-	ns	
Data Setup Time	Tdsu	5	-	-	ns	D0[7:0],D1[7:0],D2[7:0] to DCLK
Data Hold Time	Tdhd	5	-	-	ns	D0[7:0],D1[7:0],D2[7:0] to DCLK
DEN Setup Time	Tesu	5	-	-	ns	
DEN Hold Time	Tehd	5	-	-	ns	

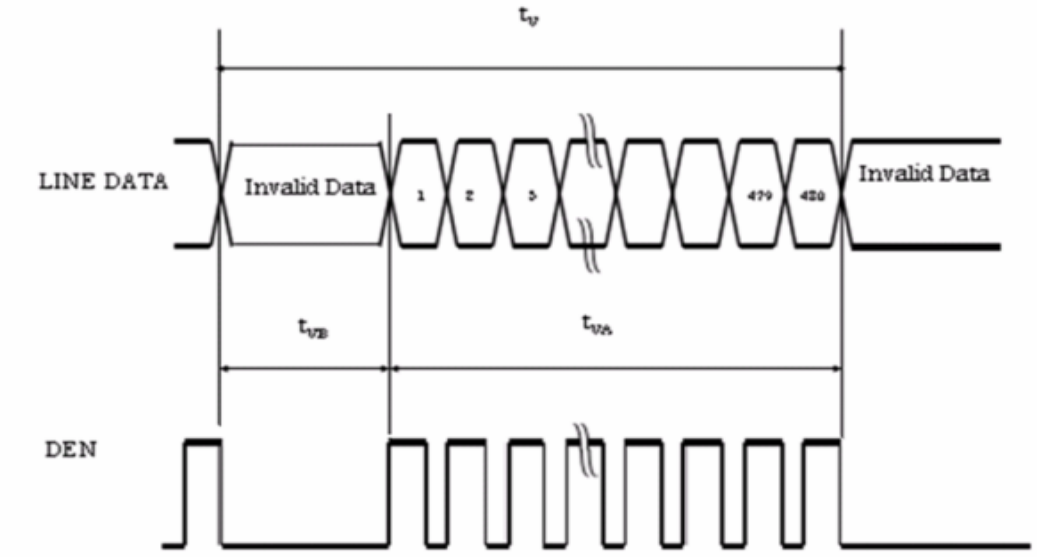


DE Mode

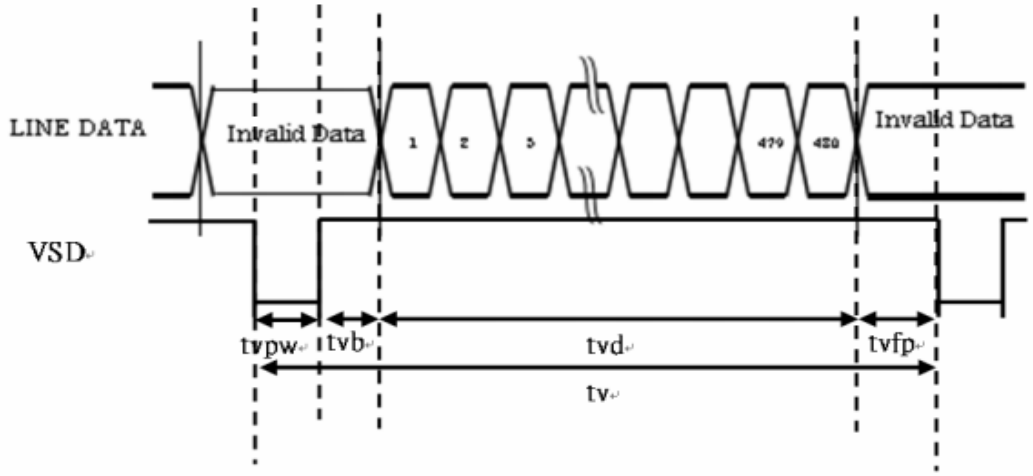
Horizontal timing：



Vertical timing：

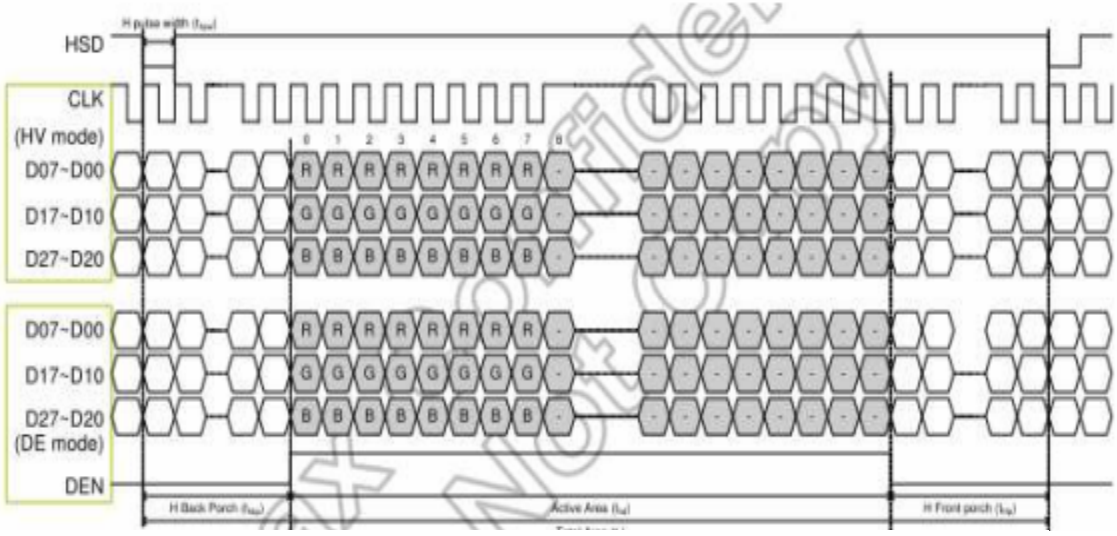


Vertical timing：

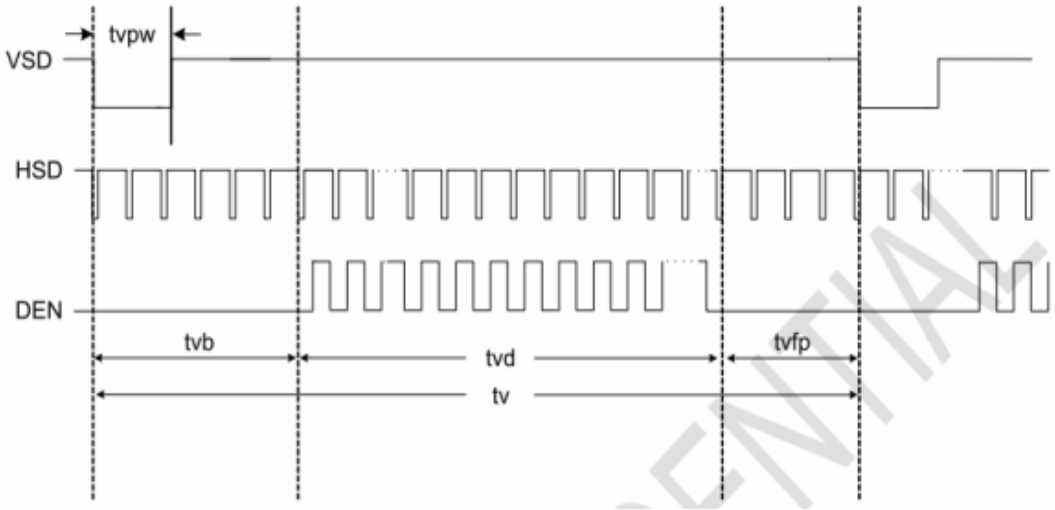


Data Input Format

Horizontal timing：

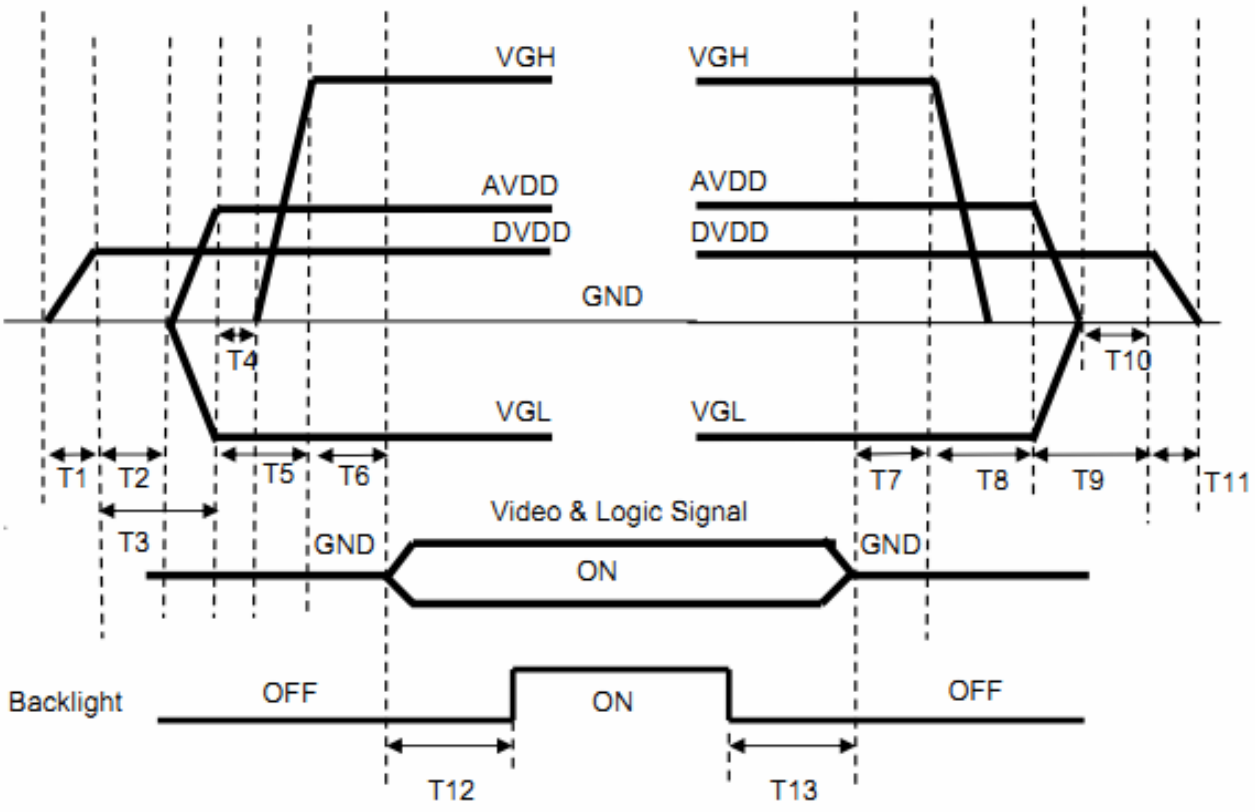


Vertical timing：



5.3 Power、Signal sequence

Power On：DVDD→AVDD/VGL →VGH →Video &Logic Signal→Backlight
Power Off：Backlight→Video &Logic Signal→ VGH→AVDD/VGL→DVDD



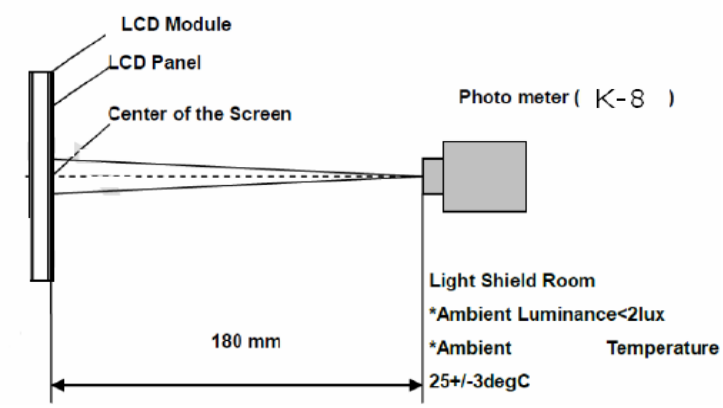
0<T1≦10ms
T2>0ms
T3>20ms
T4>0ms
T5>10ms
0<T6≦10ms
T12≧200ms

T7>0ms
T8>0ms
T9>0ms
T10>0ms
0<T11≦10ms
T13≧200ms

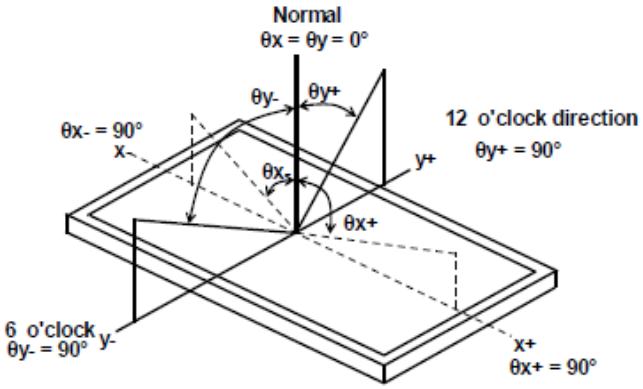
6.0 ELECTRO-OPTICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Luminance		L	θ =φ 0°	350	400	--	cd/m2	Note1
Transmittance		L	θ =φ 0°	--	4.5	--	%	Note5
Contrast Ratio		CR	Point-5	--	800	--	-	Note3
Response Time		Rr+Tf	Point-5	--	25	--	ms	Note4
Viewing Angle K=Contrast Ratio>10	Horizontal	Θ L	CR > 10	--	85	--		Note2
		Θ R		--	85	--		
	Vertical	Θ U		--	85	--		
		Θ D		--	85	--	.	
Color Chromaticity	White	X	θ =φ 0°	**0.260**	**0.310**	**0.360**		Note1
		Y		**0.280**	**0.330**	**0.380**		
	Red	X	θ =φ 0°	TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
	Green	X	θ =φ 0°	TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
	Blue	X	θ =φ 0°	TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
Color gamut (NTSC ratio)					TBD			
Color Temperature					TBD			

Note 1 :Measure condition :25° c±2° c,60±100%RH,under 10 Lux in the dark room. K-8,Viewing angle 2° .Measurement after lighting on 10 minus



Note2: Definition of Viewing Angle

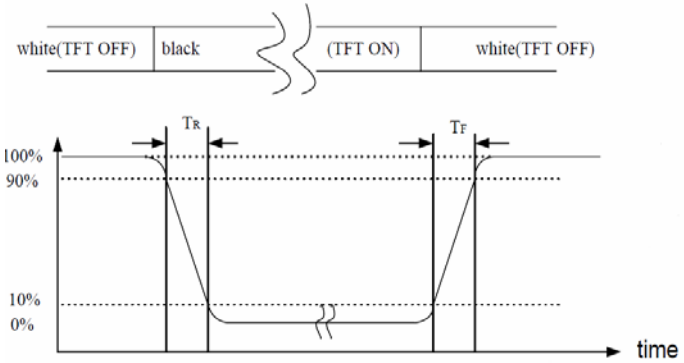


Note3： Definition of contrast ratio:

The contrast ratio can be calculated by the following expression
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note4: Definition of response time



Note (5) Definition of Transmittance(Module is without signal input)
Transmittance= Center Luminance of LCD/ Center Luminance of Back Light x100%

7.0 RELIABILITY

7.1 MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

7.2 TESTS

NO.	Test Item	Test condition	Criterion
1	High Temperature Storage	60℃±2℃ 96H Restore 2H at 25℃ Power off	
2	Low Temperature Storage	-10℃±2℃ 96H Restore 2H at 25℃ Power off	
3	High Temperature Operation	50℃±2℃ 96H Restore 2H at 25℃ Power on	
4	Low Temperature Operation	0℃±2℃ 96H Restore 2H at 25℃ Power on	
5	High Temperature & Humidity Operation	50℃±2℃ 90%RH 96H Power on	
6	Temperature Cycle	-10℃←→25℃←→60℃ 30min 5min 30min after 10cycle, Restore 2H at 25℃ Power off	Aftertesting,cosmetic and electrical defects should not happen.
7	Vibration Test	10Hz~45Hz, 100m/s2, 120min	
8	Shock Test	Half-sinewave,300m/s2,11ms	
9	Drop Test(package state)	800mm, concrete floor,1corner, 3edges, 6 sides each time	1.After testing, cosmetic and electrical defects should not happen. 2.the product should remain at initial place 3.Product uncovered or package broken is not permitted.
10	Electro Static Discharge Test (non-operation)	150pF，330Ω，Contact:±4KV,Air:±8KV Measure point :LCD glass and metal bezel 200pF，0Ω，±200V contact test Measure point :IF connector pins	IEC61000-4-2：2001 GB/T17626.2-2006

8.0 INSPECTION STANDARDS

8.1 Purpose

This incoming inspection standard shall be applied to TFT-LCD supplied by ZHONGSHEN to its customer.

8.2 Scope

This inspection standard contains Cosmetic Specifications and Electrical Specifications.

8.3 Classification of defects

9.3.1 Major defect.

The major defect is a defect that is likely to result in product failure or reduction in

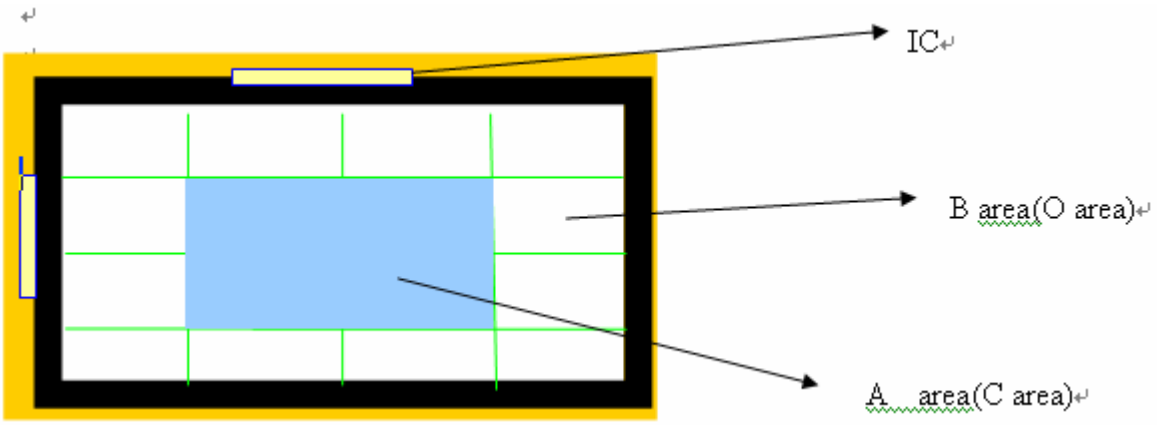
Product's intended usage.

9.3.2 Minor defect.

The minor defect is a defect that has little bearing on the effective use or Operation of the product.

8.4 Definition

9.4.1 Display area definition



8.conditions is as follows

8.5.1 Viewing distance is approximately 35-40 cm

8.5.2 Viewing angle is normal to the LCD panel as 45°

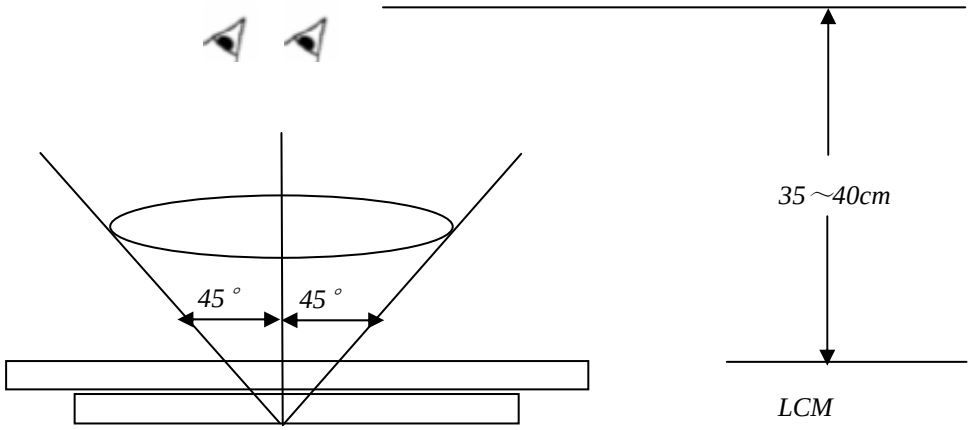
8.5.3 Ambient temperature is approximately 25±5℃

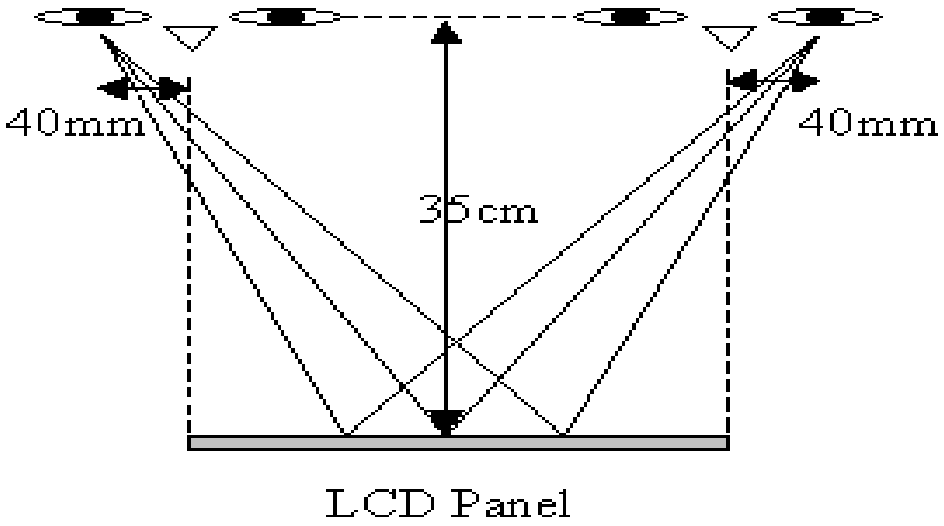
8.5.4 Ambient humidity is 60±5% RH

8.5.5 Ambient luminance is from 350-400 Lux.

8.5.6 Input signal timing should be typical value(3s-5s).

8.5.7 Mura & Light leakage inspection at ND-Filter 6%.





8.6 Sampling method

8.6.1 According to the MIL-STD-105E general inspection level , Ⅱ Sampling plan.

8.6.2 AQL: MA 0.65 MI 1.0

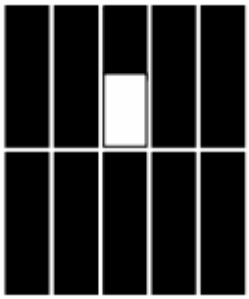
8.7 Inspection Criteria

DEFECT TYPE			LIMIT			Defect	Note
VISUAL DEFECT	SCRATCH		W≤0.05mm and L≤5mm		Ignore	Maj	NOTE1
			0.05mm<W≤0.2mm L≤10mm		N≤4		
			10mm<L, 0.1mm<W		N=0		
	INTERNAL	SPOT	Φ≤0.2mm		Ignore		
			0.2mm<Φ≤0.5mm		N≤4		
			Φ>0.5mm		N=0		
		FIBER	0.1mm≤W≤0.2mm L≤2.5mm		N≤4		
			0.2mm<W, 2.5mm<L		N=0		
		POLARIZER BUBBLE	Φ≤0.25mm		Ignore		
			0.25mm<Φ≤0.5mm		N≤4		
			Φ>0.5mm		N=0		
		DENT	Φ<0.25mm		Ignore		
			0.25mm≤Φ≤0.5mm		N≤4		
			Φ>0.5mm		N=0		
ELECTRICAL DEFECT	BRIGHT DOT		C Area	O Area	Total	Maj	NOTE2 NOTE3
			N≤4（contain C area and O area）		N≤4		
	DARK DOT		N≤5（contain C area and O area）		N≤5		
	TWO ADJACENT DOT		N≤1	N≤2	N≤3		
	THREE OR MORE ADJACENT DOT		NOT ALLOWLED				
	LINE DEFECT		NOT ALLOWLED				

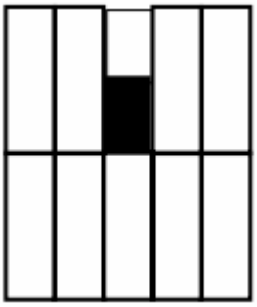
Note1: Minimum distance between dot defects and spot is 5mm;

Note2: The definition of Bright dot and Dark dot

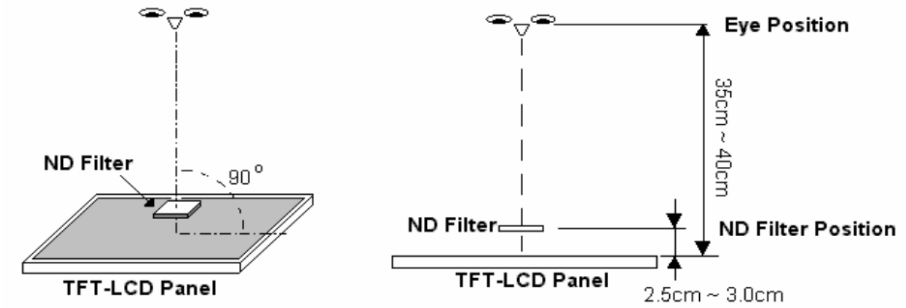
-bright area is more than 50% of one dot



-dark area is more than 50% of one dot



-The bright dot shall be visible under ND-Filter 5% as following:



NOTE3:

-A bit rate(bright dot model)≤10%;

-Class Chipping but not affect the function of quality OK;

-Polarizing film appearance does not affect the function OK;