宇华国际科技有限公司
YuHua INT,L Technology Co., LIMITED

SPECIFICATION FOR LCD MODULE

Customer : _____

Product Model: _____

Sample code: YH075WVFSN001

Designed by	Checked by	Approved by

Final Approval by Customer

☐ **LCM Machinery OK** Checked By _____ ☐ **LCM Display OK** Checked By _____	☐ **LCM OK** ☐ **NG，Problem survey:** Approved By _____

※The specification of "TBD" should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

Revision History

Date	Rev. No.	Page	Summary
2023.07.10	V1.0	ALL	FIRST ISSUE

常 备 库 存 Stock For Sale		长 期 供 货 Long Time supply	支持小量 NO MOQ	品 种 齐 全 In Full Range

Contents

	常 备 库 存 Stock For Sale	长 期 供 货 Long Time supply	支持小量 NO MOQ	品 种 齐 全 In Full Range

1. Over View

YH075WVFSN001isanActiveMatrixElectrophoreticDisplay(AMEPD),withinterfaceand a reference system design. The7.5” active area contains 800×480 pixels, andhas 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

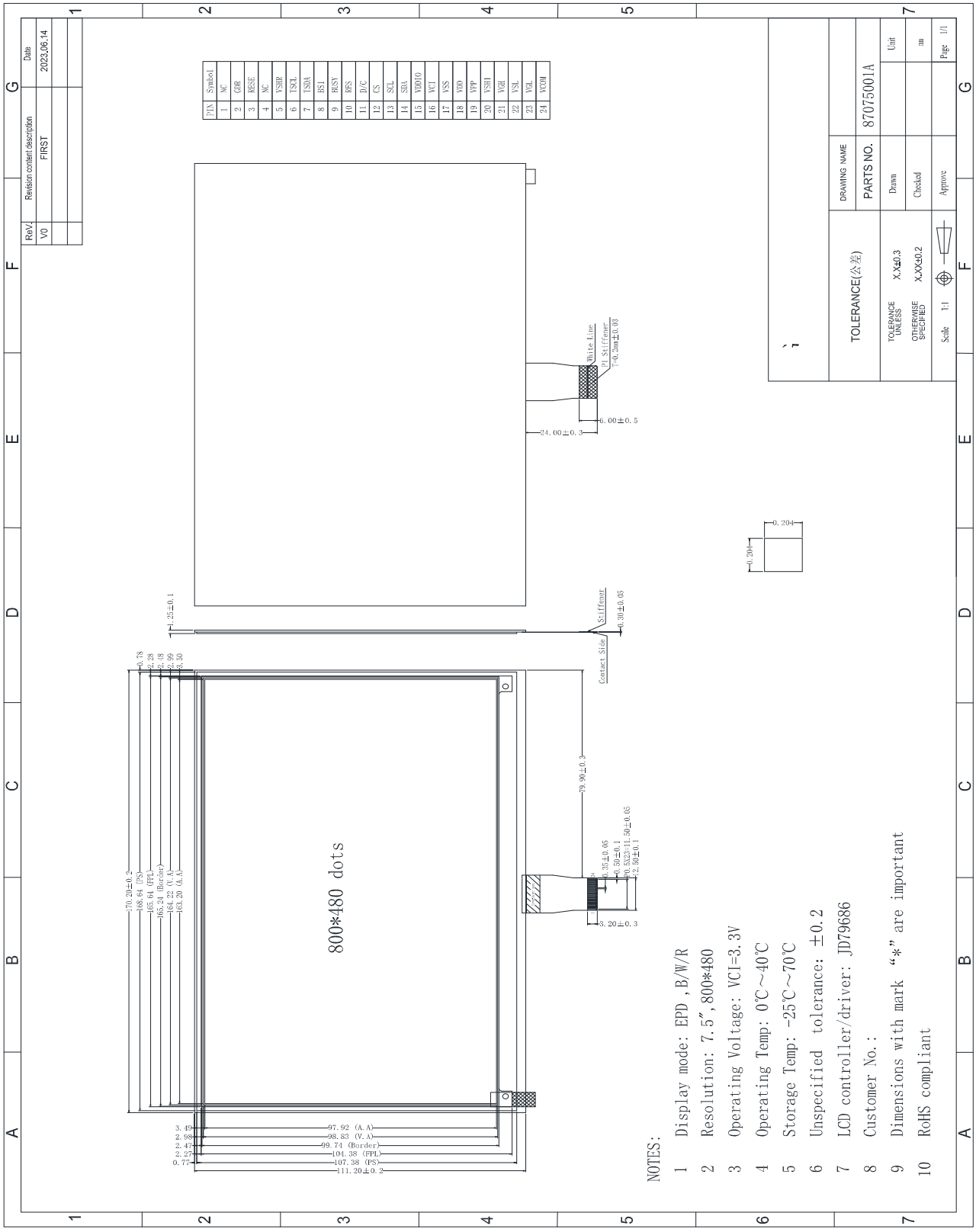
2. Features

- 800×480 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in flash memory
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C Signal Master Interface to read external temperature sensor/ built-in temperature sensor
- Available in COG package IC thickness 280um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	800(H) x 480(V)	Pixel	
Active Area	163.2(H) x 97.92(V)	mm	
Pixel pitch	0.204(H) x 0.204(V)	mm	
Pixel Configuration	Square		
Outline Dimension	170.2(H) x 111.2(V) x 1.25(D)	mm	
Module Weight	44	g	
Controller IC	JD79686		
Interface	3Wire / 4Wire SPI	-	
Display mode	EPD,B / W / R	-	
Operating temperature	0～+40	℃	
Storage temperature	-25～+70	℃	

4. Mechanical Drawing of EPD module



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5. Input/Output Pin Assignment

NO.	Name	DISCRIPTION	I/O	Remark
1	NC	NO Connection	-	Keep open
2	GDR	N-Channel MOSFET Gate Drive Control	O	
3	RESE	Current Sense Input for the Control Loop	I	
4	NC	NO Connection	-	Keep open
5	VSHR	Positive Source driving voltage(Red)	C	
6	TSCL	IIC Interface to digital temperature sensor Clock pin	O	
7	TSDA	IIC Interface to digital temperature sensor Data pin	I/O	
8	BS1	Bus Interface selection pin	I	Note 5-5
9	BUSY	Busy state output pin	O	Note 5-4
10	RES	Reset signal input. Active Low.	I	Note 5-3
11	D/C	Data /Command control pin	I	Note 5-2
12	CS	Chip select input pin	I	Note 5-1
13	SCL	Serial Clock pin (SPI)	I	
14	SDA	Serial Data pin (SPI)	I/O	
15	VDDIO	Power Supply for interface logic pins It should be connected with VCI	P	
16	VCI	Power Supply for the chip	P	
17	VSS	Ground	P	
18	VDD	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	C	
19	VPP	FOR TEST	P	
20	VSH1	Positive Source driving voltage	C	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH1	C	
22	VSL	Negative Source driving voltage	C	
23	VGL	Power Supply pin for Negative Gate driving voltage VCOM and VSL	C	
24	VCOM	VCOM driving voltage	C	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output),
P = Power Pin, C =Capacitor Pin

Note 5-1: This pin (CS) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS is pulled Low.

Note 5-2: This pin (D/C) is Data/Command control pin connecting to the MCU in 4 -wire SPI mode. When the pin is pulled High, the data at SDA will be interpreted as data. When the pin is pulled Low, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +6.0	V
Logic Input voltage	VIN	-0.5 to VCI+0.5	V
Operating Temp range	TOPR	0 to +40	ºC
Storage Temp range	TSTG	-25 to+70	ºC
Optimal Storage Temp	TSTGo	23±2	ºC
Optimal Storage Humidity	HSTGo	55±10	%RH

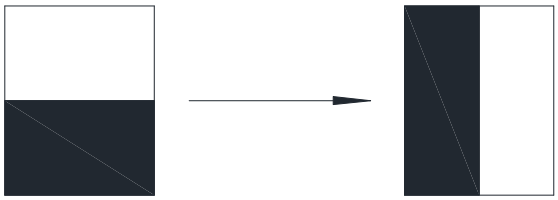
Note: Maximum ratings are those values beyond which damages to the device may occur.
Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.5	3.3	3.6	V
Core logic voltage	V_{DD}		VDD	2.5	3.3	3.6	V
High level input voltage	V_{IH}	-	-	0.7V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.3V_{CI}	V
High level output voltage	V_{OH}	IOH = -400uA	-	VCI-0.4	-	-	V
Low level output voltage	V_{OL}	IOL = 400uA	-	-	-	0.4	V
Typical power	P_{TYP}	VCI =3.3V	-	-	TBD	-	mW
Deep sleep mode	P_{STPY}	VCI =3.3V	-	-	0.71	-	mW
Typical operating current	Iopr_V_{CI}	VCI =3.3V	-	-	TBD	-	mA
Image update time	-	25 ºC	-	-	12	-	sec
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	2	5	uA

Notes:1.The typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.



2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

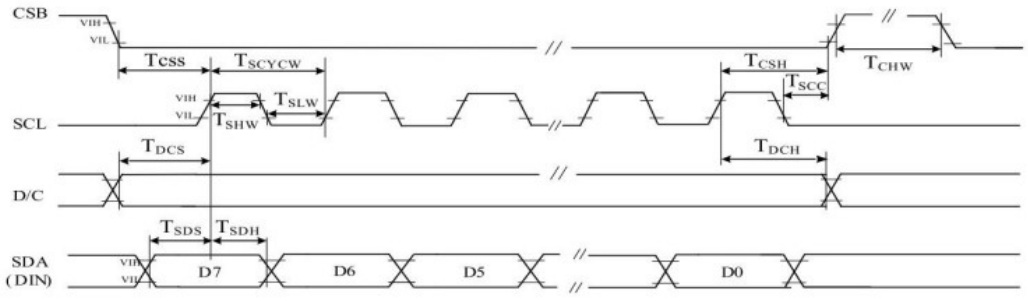
6.3 AC Characteristics

6.3.1 MCU Interface selection

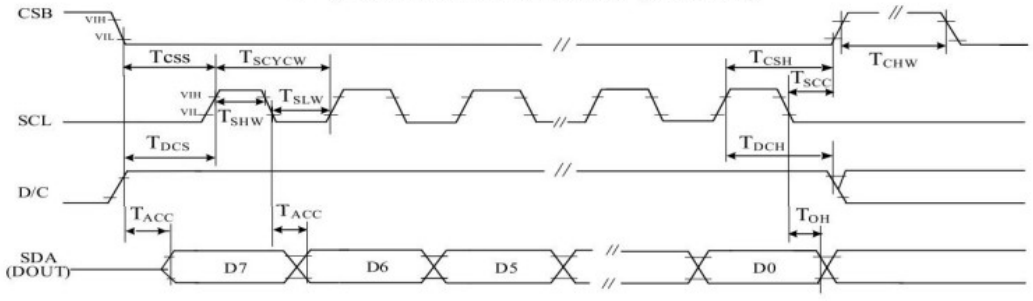
The pin assignment at different interface mode is summarized in Table.Different MCU mode can be set by hardware selection on BS1 pins.The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CSB	D/C	RSTN
BS1=L 4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
BS1=H 3-wire SPI	SDIN	SCLK	CSB	L	RSTN

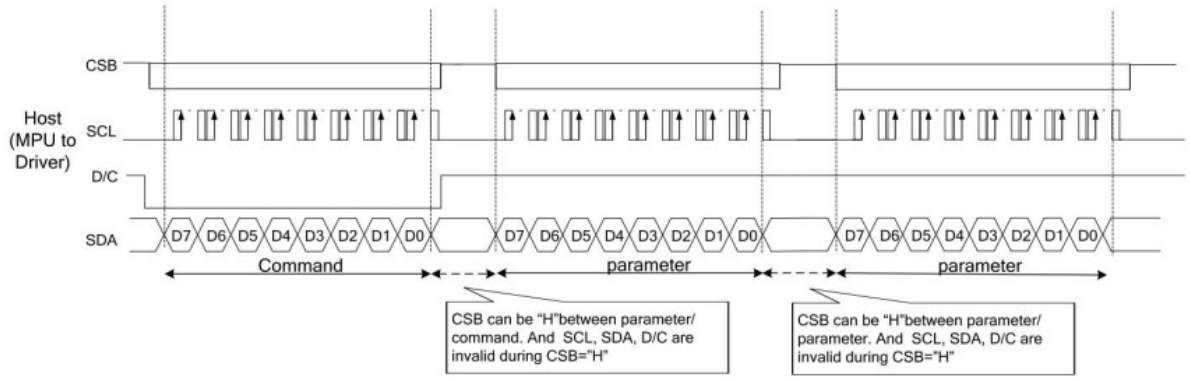
6.3.2 MCU Serial Interface (4-wire SPI)



4 pin serial interface characteristics (write mode)



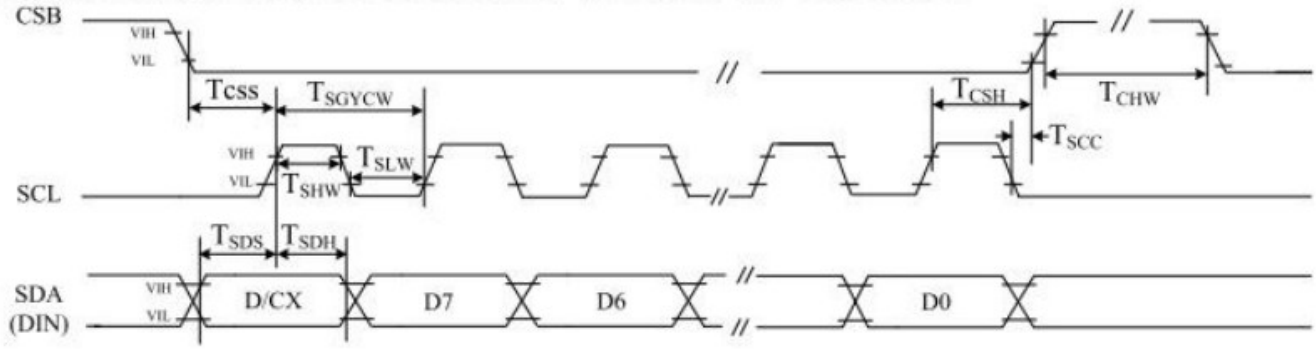
4 pin serial interface characteristics (read mode)



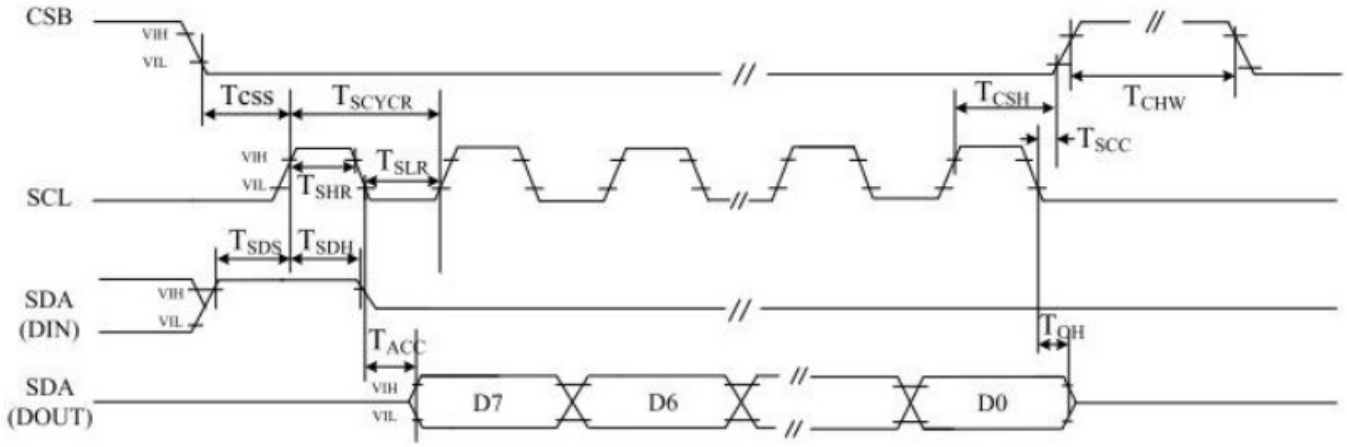
6.3.3 MCU Serial Interface (3-wire SPI)

3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. JD79686 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

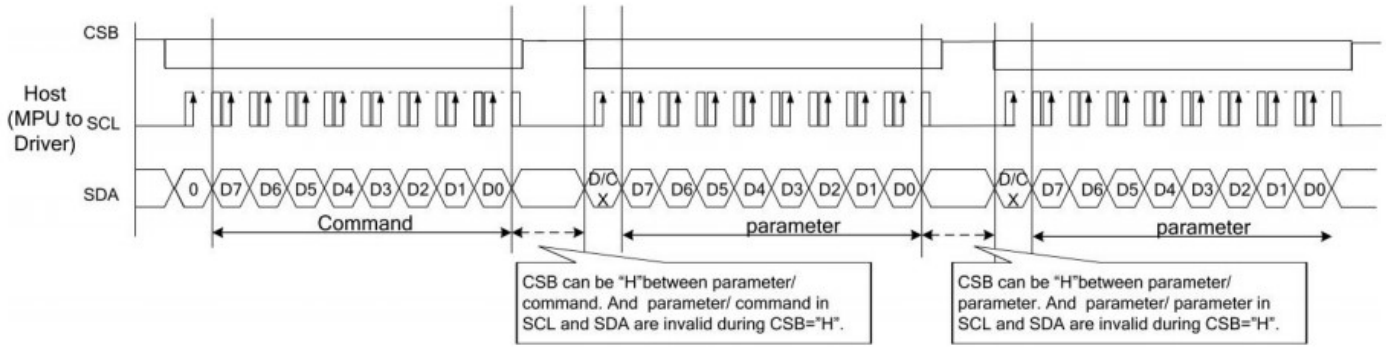
Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".



3 pin serial interface characteristics (write mode)

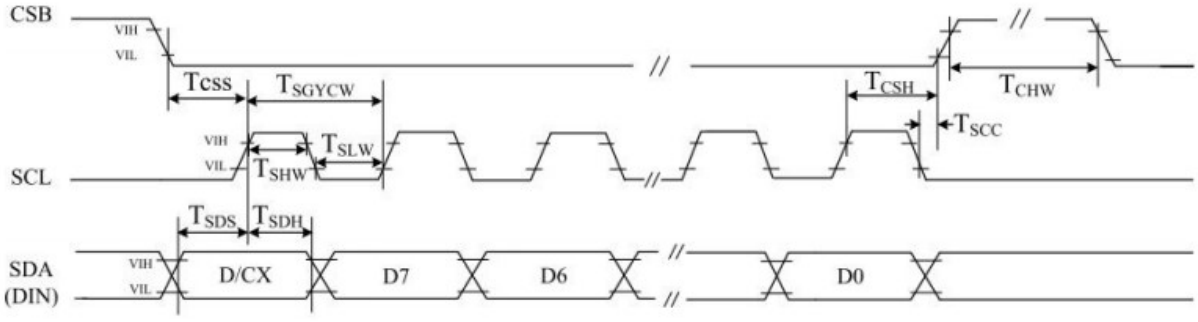


3 pin serial interface characteristics (read mode)

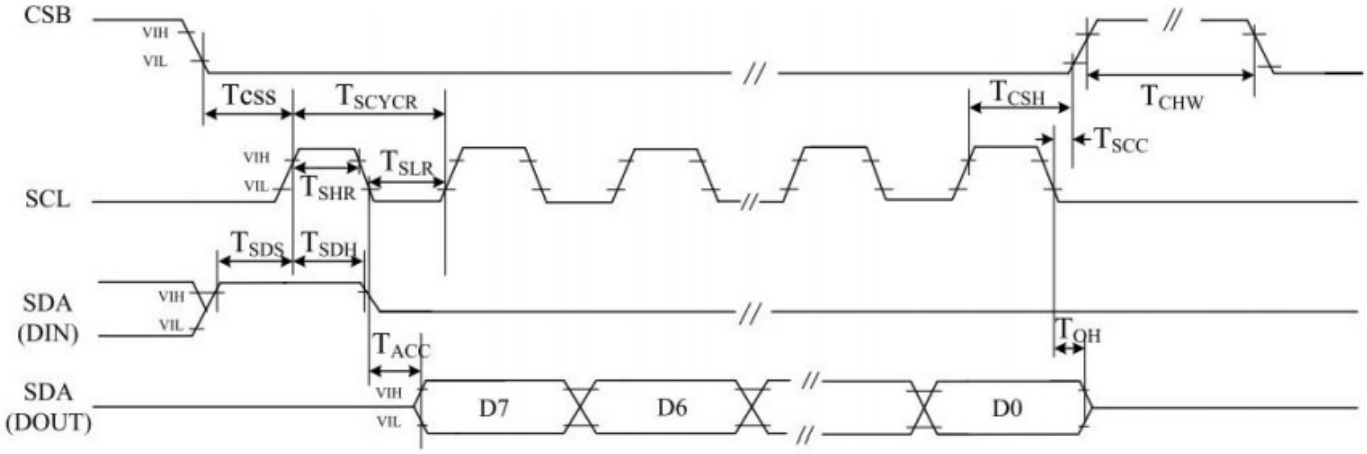


6.3.4 Interface Timing

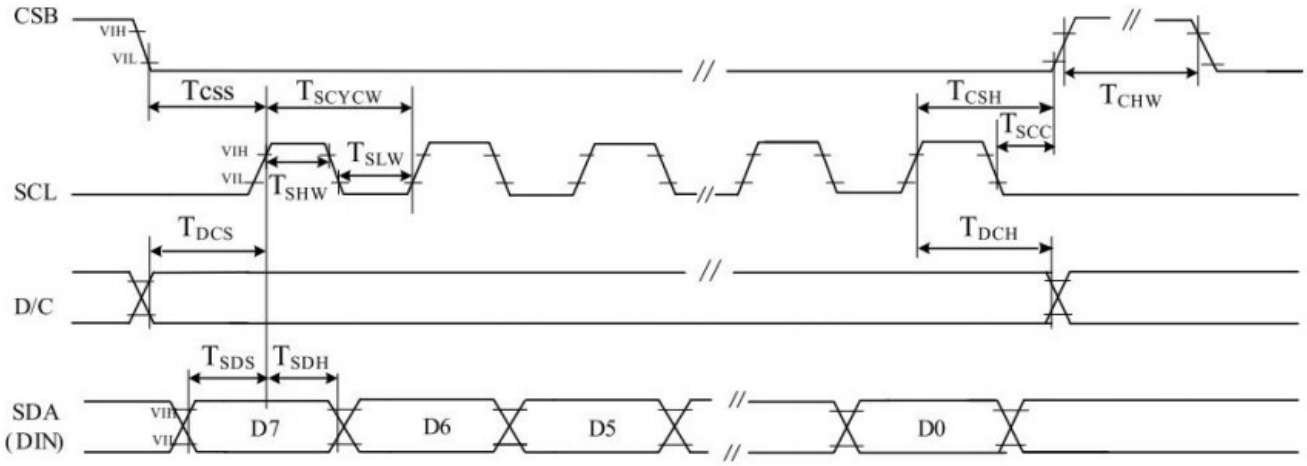
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	100			ns	Chip select setup time
	T_{CSH}	100			ns	Chip select hold time
	T_{SCC}	50			ns	Chip select CSB setup time
	T_{CHW}	500			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35	-		ns	SCL "H" pulse width (Write)
	T_{SLW}	35	-		ns	SCL "L" pulse width (Write)
	T_{SCYCR}	200	-		ns	Serial clock cycle (Read)
	T_{SHR}	85			ns	SCL "H" pulse width (Read)
	T_{SLR}	85			ns	SCL "L" pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}	10			ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time
RC loading						
Source driver output loading	RL_S	-	11.95k		Ω	
	CL_S	-	42		pf	
Gate driver output loading	RL_S		37.3k		Ω	
	CL_S		170pf		pf	
VCOM output loading	RL_com		2.85 k		Ω	
	CL_com		2300		pf	
Driver						
Source driver rise time	trS		5		us	99% final value
Source driver fall time	tFS		5		us	
Gate driver rise time	TrG		5		us	99% final value
Gate driver fall time	tFG		5		us	
VCOM rise time	trCOM		1		ms	99% final value
VCOM fall time	tFCOM		1		ms	



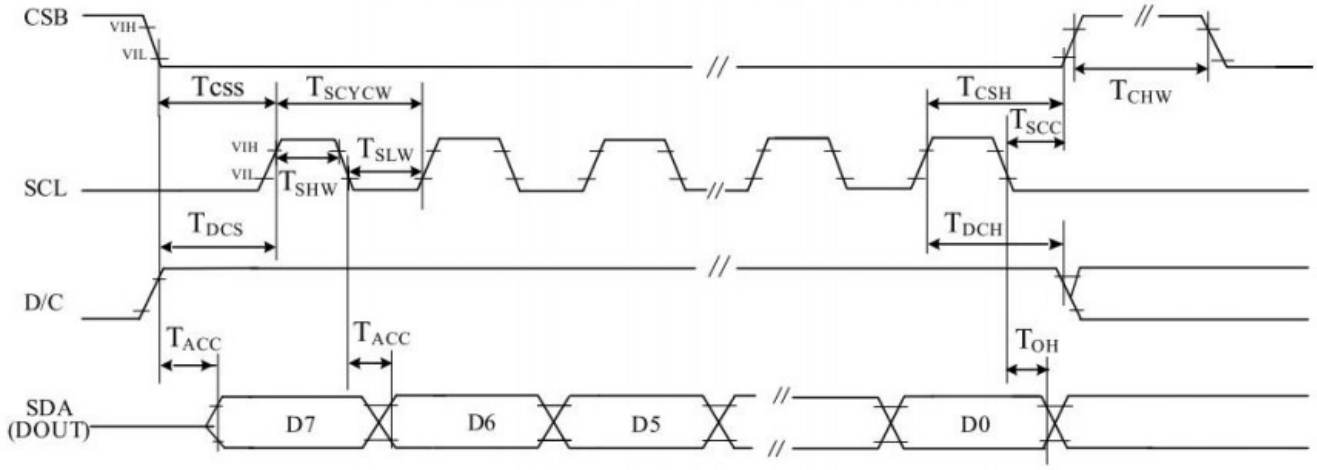
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)

7. Optical Characteristics

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	7-1
CR	Contrast Ratio		8.1		-	-	7-2
GN	2Grey Level	-	-	DS+(WS-DS)* n(m-1)			7-3
T update	Image update time	at 25 °C	-	12	-	ms	

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

7-3. WS: White state, DS: Dark state

8. Command Table

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	-00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
		W	1			-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3Fh
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3Fh
		W	1		VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0Fh
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	T_VDS_OFF [1]	T_VDS_OFF[0]					00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
		W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
		W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
R14H	Partial Data Start transmission1 (PDTM1)	W	0	0	0	0	1	0	1	0	0	14H
		W	1	#	#	#	#	#	#	#	#	00h
R15H	Partial Data Start transmission 2 (PDTM2)	W	0	0	0	0	1	0	1	0	1	15H
		W	1	#	#	#	#	#	#	#	#	00h
R16H	Partial Display Refresh(PDRF)	W	0	0	0	0	1	0	1	1	0	16H
		W	1	#	#	#	#	#	#	#	#	00h
R20H	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
R21H	White to White LUT (LUTWW)	W	0	0	0	1	0	0	0	0	1	21H
		W	1	#	#	#	#	#	#	#	#	00h
R22H	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00h
R23H	White to Black LUT (LUTWB/LUTW)	W	0	0	0	1	0	0	0	1	1	23H
		W	1	#	#	#	#	#	#	#	#	00h
R24H	Black to Black LUT	W	0	0	0	1	0	0	1	0	0	24H

	(LUTBB/LUTB)	W	1	#	#	#	#	#	#	#	#	00h
R25H	LUTC option	W	0	0	0	1	0	0	1	0	1	25H
		W	1							XON [9:8]		00h
		W	1	XON [7:0]								00h
		W	1							ST_CHV [9:8]		00h
		W	1	ST_CHV [7:0]								00h
R26H	Set Vcom/Red states	W	0	0	0	1	0	0	1	1	0	26H
		W	1	0	0			vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h
R30H	OSC control (OSC)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-		M[2:0]			N[2:0]			3Ah
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	--
		R	1	D2	D1	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	-
R60H	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
		W	1	-	-	-	-	-	-	-	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R62H	Source & gate start setting	W	0	0	1	1	0	0	0	1	0	62H
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	-	-	-	00h
		W	1				gscan				G_start [8]	00h
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-
		R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV10]	REV[09]	REV[08]	-
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	-	PTL_flag	I²C_ERR	I²C_ BUSYN	Data_flag	PON	POF	BUSY_N	-
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	-	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	1Fh
RA0H	Program Mode (PGM)	W	0	1	0	1	0	0	0	0	0	A0H
		W	1	1	0	1	0	0	1	0	1	A5h
RA1H	Active program(APG)	W	0	1	0	1	0	0	0	0	1	A1H

RA2H	Read OTP Data (ROTP)	W	0	1	0	1	0	0	0	1	0	A2H
		R	1	#	#	#	#	#	#	#	#	-
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h
RE6H	LVD voltage Select	W	0	1	1	1	0	0	1	1	0	E6H
		W	1	-	-	-	-	-	-	LVD_SEL[1]	LVD_SEL[0]	11h
RE7H	Panel Break Check	W	0	1	1	1	0	0	1	1	1	E7H
		R	1	-	-	-		-	-	-	PSTA	-
RE8H	Power saving	W	0	1	1	1	0	1	0	0	0	E8H
		W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h
RE9H	AUTO sequence	W	0	1	1	1	0	1	0	0	1	E9H
		W	1	1	0	1	0	0	1	0	1	00h
REBH	OTP LUT backup1 program	W	0	1	1	1	0	1	0	1	1	EBH
RECH	Read OTP LUT backup1	W	0	1	1	1	0	1	1	0	0	ECH
		R	1	#	#	#	#	#	#	#	#	–
REDH	OTP LUT backup2 program	W	0	1	1	1	0	1	1	0	1	EDH
		R	1	#	#	#	#	#	#	#	#	–
REEH	Read OTP LUT backup2	W	0	1	1	1	0	1	1	1	0	EEH
REFH	Checksum Program to OTP	W	0	1	1	1	0	1	1	1	1	EFH
RF0H	Remap LUT	W	0	1	1	1	1	0	0	0	0	F0H
		W	1	-	-	-	bkup_lut_2_en	rmp2_table_sel[3]	rmp2_table_sel[2]	rmp2_table_sel[1]	rmp2_table_sel[0]	1Fh
		W	1	-	-	-	bkup_lut_1_en	rmp1_table_sel[3]	rmp1_table_sel[2]	rmp1_table_sel[1]	rmp1_table_sel[0]	1Fh
RF1H	Set OTP program	W	0	1	1	1	1	0	0	0	1	F1H
		W	1	-	-	-	-	-	-	LUT_bank	reg_bank	03h
RF2H	Read checksum	W	0	1	1	1	1	0	0	1	0	F2H
		R	1	#	#	#	#	#	#	#	#	00h
RF3H	Calculate Checksum	W	0	1	1	1	1	0	0	1	1	F3H

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh

Bit	Name	Description
0	RST_N	RST_N function 1 : no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. **(default)**
2	SHL	SHL function 0: Shift left; First data=Sn →Sn-1 → …→S2 →Last data=S1. 1: Shift right: First data=S1→ S2 → …→Sn-1 → Last data=Sn. **(default)**
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→ G2 → Last line=G1. 1:Scan up; First line=G1 →G2 →…→Gn-1 →Last line=Gn. **(default)**
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. **(default)** 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP**(default)** 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 600x448 01: Display resolution is 640x480 10: Display resolution is 720x540 11: Display resolution is 800x600 (default)

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1	-	-	-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3Fh
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3Fh
5th Parameter	W	1	-	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	**Gate power selection.** 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
1	VDS_EN	**Source power selection.** 0 : External source power from VSH/VSL pins. 1 : Internal DC/DC function for generate VSH/VSL. (default)

2nd Parameter:

Bit	Name	Description
2-0	VGHL_LV	**VGHL_LV Voltage Level.** 000: VGH=20 v, VGL=-20v (default) 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v 110: VGH=14 v, VGL=-14v 111: VGH=13 v, VGL=-13v
3	VCOM_HV	**VCOM Voltage Level** 0: VCOMH=VSH+VCOMDC,VCOML=VSL+VCOMDC(default) 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT. **(Default value: 111111b)**

Bit	Name	Description
5-0	**VSH**	**Internal VSH power selection.** 000000: 2.4 v 000001: 2.6 v 000010: 2.8 v 000011: 3.0 v ....

		010111: 7.0V 011000: 7.2 V 011001: 7.4 V .... 111010: 14.0V 111011: 14.2 V 111100: 14.4V 111101: 14.6V 111110: 14.8V 111111: 15.0V

4th Parameter: Internal VSL power selection for B/W LUT. **(Default value: 111111b)**

Bit	Name	Description
5-0	**VSL**	**Internal VSL power selection.** 000000: -2.4 v 000001: -2.6 v 000010: -2.8 v 000011: -3.0 v .... 010111: -7.0V 011000: -7.2 V 011001: -7.4 V .... 111010 :-14.0V 111011: -14.2 V 111100: -14.4 V 111101: -14.6V 111110: -14.8V 111111: -15.0V

5th Parameter: Internal VSHR power selection for Red LUT. **(Default value: 00001111b)**

Bit	Name	Description
6-0	**VSHR**	**Internal VSL power selection.** 0000000: 2.4 v 0000001: 2.5 v 0000010: 2.6 v 0000011: 2.7 v .... 0101110: 7.0 V 0101111: 7.1 V 0110000: 7.2 V .... 1010001: 10.5V 1010010: 10.6 V 1010011: 10.7 V 1010100: 10.8V 1010101: 10.9V 1010110: 11.0V

Note:
1.VSH>VSHR

Restriction	

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will keep floating.
Restriction	

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-	-	Vsh_off[1]	Vsh_off [0]	Vsl_off[1]	vsl_off[0]	vshr_off[1]	vshr_off[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : 1st Parameter:
Restriction	

Bit	Name	Description
1-0	**vshr_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
3-2	**vsl_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
5-4	**vsh_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.
Restriction	

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power d ːment. (R40H).
Restriction	

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
2nd Parameter	W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
3rd Parameter	W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	**Driving strength of phase A**	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase A**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description
2-0	**Driving strength of phase B**	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase B**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

Description	3rd Parameter: Bit 2-0 — **Minimum OFF time setting of GDR in phase C** 000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8 Bit 5-3 — **Driving strength of phase C** 000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
...	W	1									00h
Mx Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / -- / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1".

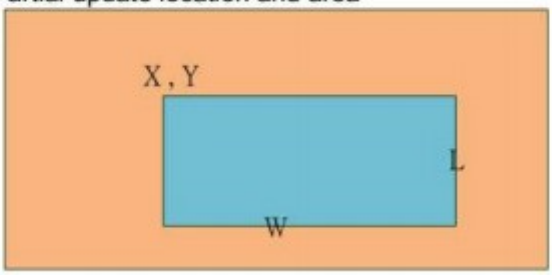
R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
...	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

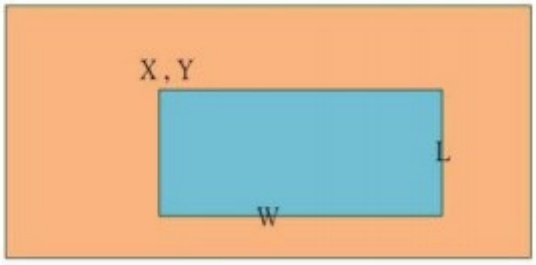
R14H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM1	W	0	0	0	0	1	0	1	0	0	14H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

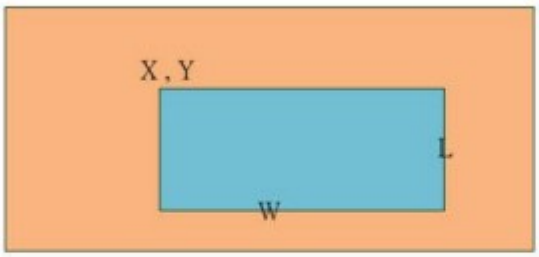
R15H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM2	W	0	0	0	0	1	0	1	0	0	15H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

R16H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDRF	W	0	0	0	0	1	0	1	1	0	16H
1st Parameter	W	1	DFV_EN						X[9]	X[8]	00h
2nd Parameter			X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter	W	1							Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	00h
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	
8th Parameter			L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT After display refresh command, BUSY_N signal will become "0".  Note: X and W should be the multiple of 8. DFV_EN: data follow VCOM function on display area. DFV_EN=1: Only effective in B/W mode, if pixel from "New data" SRAM equal to "Old data" SRAM on display area, this pixel output would follow VCOM LUT. DFV_EN=0: Data doesn't follow VCOM LUT.
Restriction	this command only active when BUSY_N = "1".

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~13th Parameter	W	1	2nd state								00h
....	W	1	3rd ~9th state								00h
55th ~60h Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This register is set for VCOM LUT. This command stores VCOM Look-Up Table with 10 states of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.
Restriction	- This command only actives when BUSY_N = "1".

define	description
Level selection [1:0]	00: -VCM_DC 01: VSH+VCM_DC. 10: VSL+VCM_DC. 11: Floating.
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame ... 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 00000001: 1 ... 11111110: 254 11111111: 255

R21H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWW	W	0	0	0	1	0	0	0	0	1	21H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
....	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
....	W	1	3rd ~9th state								00h
55th ~60th Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWB/LUTW	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
....	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
....	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

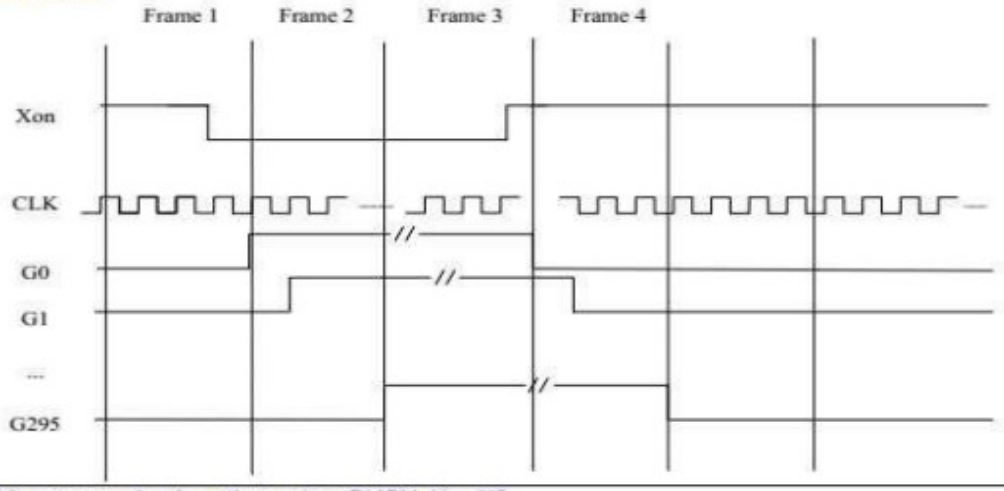
Description	- The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

R25H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC option	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1							XON [9:8]		00h
2nd Parameter	W	1	XON [7:0]								00h
3rd Parameter	W	1							VCOM_H [9:8]		00h
4th Parameter	W	1	VCOM_H [7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This register is set for VCOM LUT. XON[9:0] — All Gate ON 0000000000: No all gate on. 0000000001: State1 gate power on 1111111111: State1~10 all gate power on VCOM_H[9:0] — Control VCOM Power as High 0000000000: No VCOM High voltage 0000000001: State1 VCOM High voltage .... 1111111111: State1~10 VCOM High voltage Xon function: 
Restriction	- This command only actives when BUSY_N = "1".

R26H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_STG	W	0	0	0	1	0	0	1	1	0	H
1st Parameter	W	1			-	-	vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h

Description	This command is used to set VCOM/Red LUT states Function of vcom_stg_sel [1:0]/ b2w_stg_sel[1:0] are shown below Value — Stages 00 — 7 01 — 8 10 — 9 11 — 10 Default is set as 7 stages.
Restriction	These settings are valid for BWR mode.

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
OSC	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

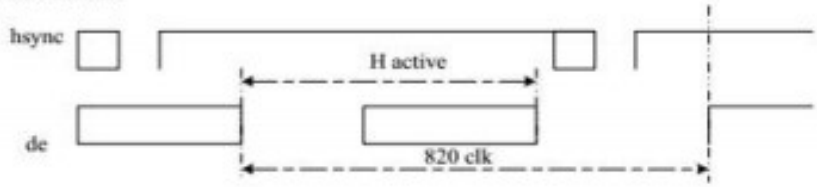
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The command controls the OSC clock frequency. The OSC structure must support the following frame rates:

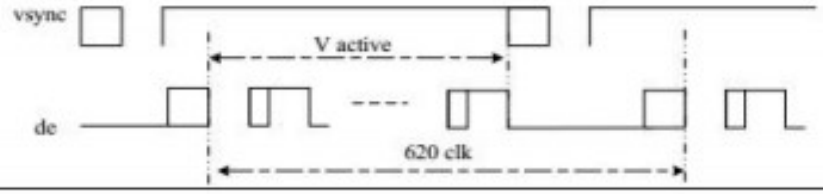
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ (default)
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark

-Horizental



-Vertical



Restriction	

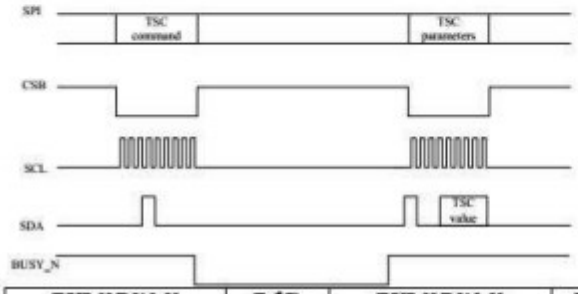
R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2	D1	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

Restriction

This command only actives after R04H(PON) or R05H(PMES)

Description	-The command defines as: This command indicates the driver IC temperature sensor enable and calibration function. **Bit** / **temperature** 2-0: mean temperature offset value 000:0℃ 001:1℃ 010:2℃ .... 111:7℃ 3: Positive and negative value 0:"+" 1: "-" 7: **Internal temperature sensor enable** 0: Internal temperature sensor enable.(**default**) 1: Internal temperature sensor disable, using external temperature sensor. For example: 1100: - 4 degree c 0111: + 7 degree c
Restriction	This command only actives after R04H(PON) or R05H(PMES)

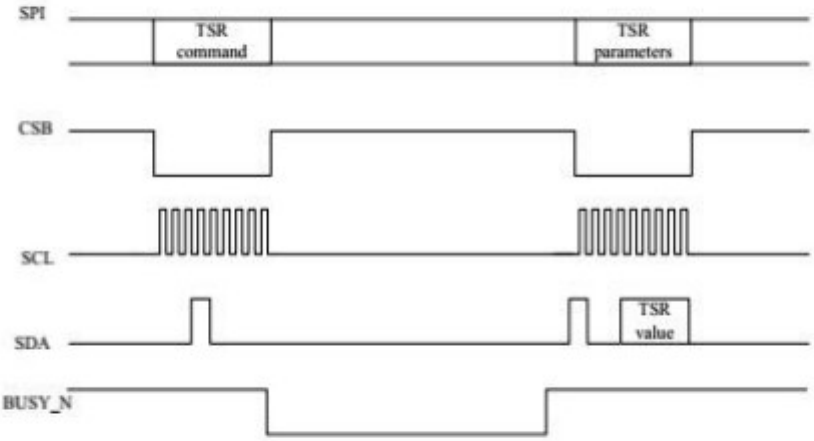
R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command writes the temperature. 1st Parameter: **Bit** / **temperature** 2-0: Pointer setting 5-3: User-defined address bits (A2, A1, A0) 7-6: I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter) 2nd Parameter: **Bit** / **temperature** 7-0: MSByte of write-data to external temperature sensor 3nd Parameter: **Bit** / **temperature** 7-0: LSByte of write-data to external temperature sensor
Restriction	This command only actives after R04H(PON) or R05H(PMES)

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

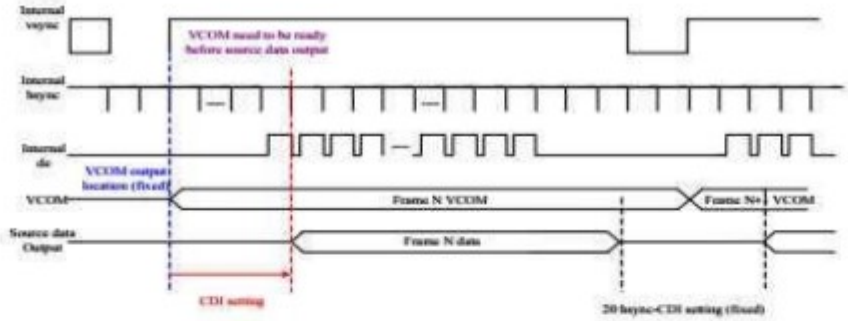
Description	-The command defines as: This command reads the temperature sensed by the temperature sensor. 1st Parameter: **Bit** | **temperature** 7-0 | MSByte of read-data from external temperature sensor 2nd Parameter: **Bit** | **temperature** 7-0 | LSByte of write-data from external temperature sensor 
Restriction	This command only actives after R04H(PON) or R05H(PMES)

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: 1st Parameter: CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	
3-0	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0] Border data selection.

B/W/Red mode(BWR=0)

Bit 5-4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 5-4	Bit7-6	description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (1->0)
	10	LUTBW (0->1)
	11	Floating

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)

Bit 5-4	Description	
DDX[1:0]	Data (Red, B/W)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

Bit 5-4	Description	
DDX[0]	Data (New,Old)	LUT
0	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
1 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE6H (LVSEL)). 1st Parameter:

Bit 0	LPD
0	Low power input.
1	Normal status.

Restriction	

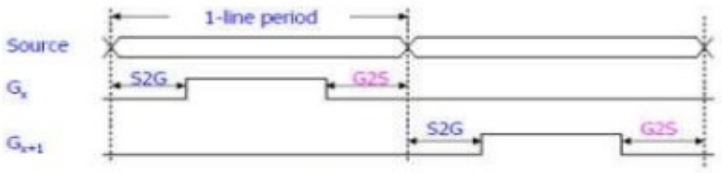
R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command define Non-overlap period of gate and source as below: 1st Parameter:

Bit	Period
S2G[3:0]/G2S[3:0]	0000: 2 clock(default) 0001: 4 clock 0010: 6 clock 0011:8 clock 0100: 10 clock 0101: 12 clock 0110: 14 clock 0111: 16 clock 1000: 18 clock 1001: 20 clock 1010: 22 clock 1011: 24 clock 1100: 26 clock 1101: 28 clock 1110: 40 clock 1111: 32 clock

Period=660ns



1 line times=1 frame times/620 line(max.gate(600 lines)+fix blanking(20 lines)
Gate on time= 1 line times-gate off time(S2G+G2S times)

Restriction	

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1	-		I²C_ERR	I²C_BUSYN	Data_flag	PON	POF	BUSY_N	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the IC status. Host can read this data to understand the IC status. 1st Parameter:

Bit	Function
5	I2C master error status
4	I2C master busy status (low active)
3	Driver has already received one frame data
2	PON 0: Not in PON mode 1: In PON mode
1	POF 0: Not in POF mode(default) 1: In POF mode
0	Driver busy status(low active)

Restriction	User can send this command in any time. It doesn't have restriction of BUSY_N.

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80 H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the IC status. Host can read this data to understand the IC status. 1st Parameter:

Bit	Function
0	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
3	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s

Restriction	This command only actives when BUSY_N = "1".

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command could get the Vcom value 1st Parameter: Bit: 5-0 — Function: Vcom value 000000: -0.1V 000001:-0.15V 000010:-0.2V 111000:-2.9V 111001:-2.95V 111010:-3.0V
Restriction	This command only actives when BUSY_N = "1".

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	1Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command set the VCOM DC value. Driver will base on this value for VCM_DC. 1st Parameter: Bit: 5-0 — Function: **VCOM value** 000000: -0.1V 000001:-0.15V 000010:-0.2V 111000:-2.9V 111001:-2.95V 111010:-3.0V
Restriction	This command only actives when BUSY_N = "1".

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code = 0xA5.
Restriction	This command only actives when BUSY_N = "1".

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

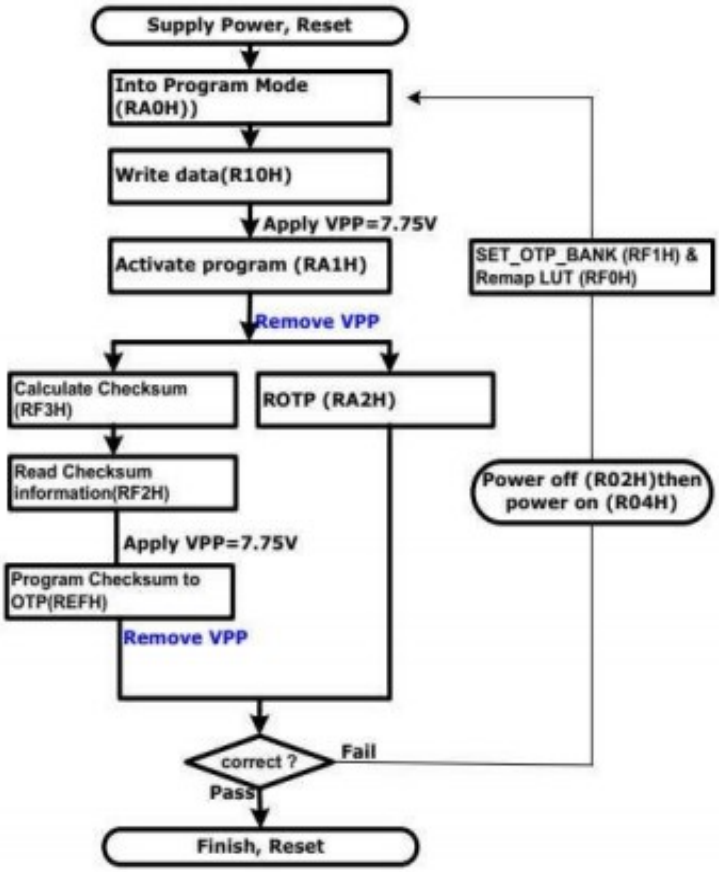
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the OTP								-
3rd Parameter	R	1	The data of address 0x001 in the OTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the OTP								-
6th~(m-1)th Parameter	R	1	.....								-
mth Parameter	R	1	The data of address (n) in the OTP								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.
Restriction	This command only actives when BUSY_N = "1".



The sequence of programming OTP

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter: **Bit** 0: Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip. 1: Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor / external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.
Restriction	This command only actives when BUSY_N = "1".

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to fix the temperature value of master and salve
Restriction	

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to fix the temperature value of master and salve
Restriction	

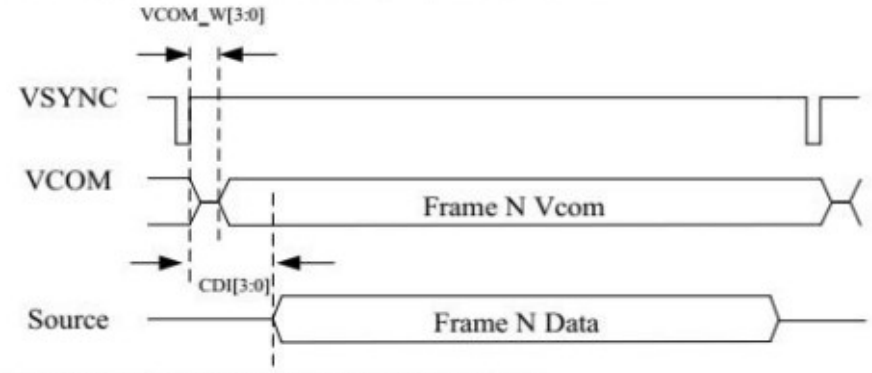
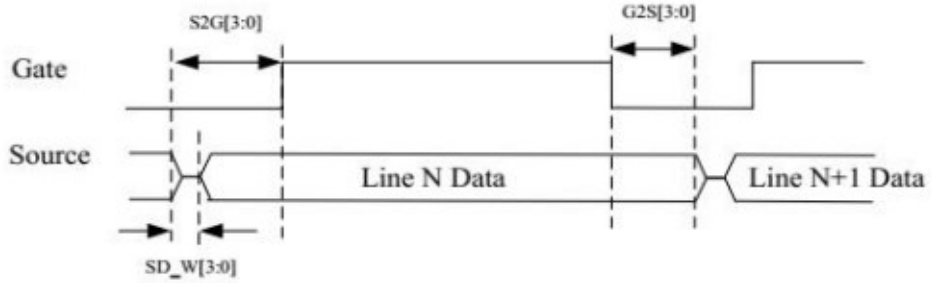
RE6H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	0	E6H
1st Parameter	W	1							LVD_SEL[1]	LVD_SEL[0]	11h

Description	LVD_SEL[1:0]: Low power Voltage selection LVD_SEL[1:0] / LVD value 00 / < 2.2 V 01 / < 2.3 V 10 / < 2.4 V 11 / < 2.5 V
Restriction	

RE7H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	1	E7H
1st Parameter	R	1								PSTA	-

Description	This command is used to enable panel check, and to disable after reading result. 1st Parameter: Bit / PSTA 0 / Panel check fail (panel broken). 1 / Panel check pass
Restriction	

RE8H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Power Saving	W	0	1	1	1	0	1	0	0	0	E8H
1st Parameter	W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h

Description	This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.1st Parameter: Vcom_W[3:0]: VCOM power saving width (unit = line period)  SD_W[3:0]: Source power saving width (unit = 660nS) 
Restriction	

RE9H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AUTO Sequence	W	0	1	1	1	0	1	0	0	1	E9H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	00h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0xE9) + Code(0xA5) = (PON->DRF->POF) AUTO (0xE9) + Code(0xA7) = (PON->DRF->POF->DSLP)
Restriction	

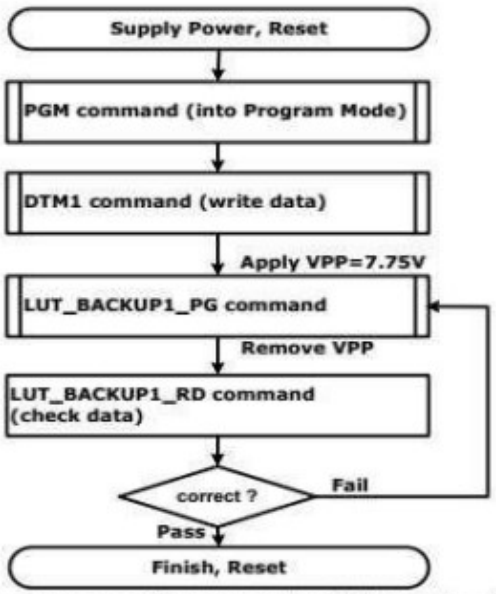
REBH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP1_PG	W	0	1	1	1	0	1	0	1	1	EBH

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

RECH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP1_RD	W	0	1	1	1	0	1	1	0	0	ECH
1st Parameter	R	1	Dummy								
2nd Parameter	R	1	The data of address 0xA00/0x1600 in the OTP								
3rd Parameter	R	1	The data of address 0xA01/0x1601 in the OTP								
4th Parameter	R	1	The data of address 0xA02/0x1602 in the OTP								
5th Parameter	R	1	The data of address 0xA03/0x1603 in the OTP								
6th~ 256th Parameter	R	1	.....								
257th Parameter	R	1	The data of address 0xAFF/0x16FF in the OTP								

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFF.  The sequence of programming OTP LUT backup1
Restriction	This command only actives when BUSY_N = "1".

REDH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP2_PG	W	0	1	1	1	0	1	1	0	1	EDH

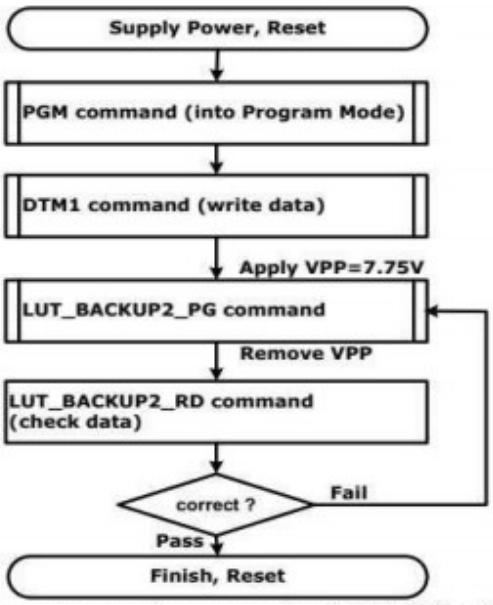
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

REEH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP2_RD	W	0	1	1	1	0	1	1	1	0	EEH
1st Parameter	R	1	Dummy								
2nd Parameter	R	1	The data of address 0xB00/0x1700 in the OTP								
3rd Parameter	R	1	The data of address 0xB01/0x1701 in the OTP								
4th Parameter	R	1	The data of address 0xB02/0x1702 in the OTP								
5th Parameter	R	1	The data of address 0xB03/0x1703 in the OTP								
6th~ 256th Parameter	R	1	.....								
257th Parameter	R	1	The data of address 0xBFF/0x17FF in the OTP								

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFF.
Restriction	This command only actives when BUSY_N = "1".



The sequence of programming OTP LUT backup2

REFH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CHKSUM_PG	W	0	1	1	1	0	1	0	1	1	EFH

Description	This command is used to Program Checksum of LUT Table
Restriction	Apply VPP to OTP before use this command

RF0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RM_LUT_CMD	W	0	1	1	1	1	0	0	0	0	F0H
1st Parameter	W	1	-	-	-	tr10_lut_en	rmp2_table_sel[3]	rmp2_table_sel[2]	rmp2_table_sel[1]	rmp2_table_sel[0]	1Fh
2nd Parameter	W	1	-	-	-	tr9_lut_en	rmp1_table_sel[3]	rmp1_table_sel[2]	rmp1_table_sel[1]	rmp1_table_sel[0]	1Fh

NOTE: "-" Don't care. can be set to VDD or GND level

2nd Parameter

tr9_lut_en :

Value	Function
1	OTP Address B00h~BFFh is used as "TR9 WF"
0	OTP Address B00h~BFFh is used as "Backup 1", And you can replace one of TR0 ~TR8.

rmp1_tab_sel[3:0]

Only be functional when tr9_lut_en is set "0", target LUTs to be replaced is shown below

Value	Target LUTs
0001	TR0
0010	TR1
0011	TR2
0100	TR3
0101	TR4
0110	TR5
0111	TR6
1000	TR7
1001	TR8
1010~1111	None

Notice :

If rmp1_tab_sel = rmp2_tab_sel , the control hardware will reload "backup 1" block to replace target LUT.

Restriction

RF1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_OTP_BANK	W	0	1	1	1	1	0	0	0	1	F1H
1st Parameter	W	1			-	-	-	-	LUT_bank0	reg_bank0	03h

Description

This command is used to set program bank for registers and LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h~BFFh	LUTs	D00h~17FFh	LUTs

reg_bank :

Value	Function
1	Program "Temp. segment" and "Default Setting" in bank 0
0	Program "Temp. segment" and "Default Setting" in bank 1

LUT_bank :

Value	Function
1	Program "LUTs" in bank 0
0	Program "LUTs" in bank 1

Restriction

RF2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RD_CHKSUM	W	0	1	1	1	1	0	0	1	0	F2H
1st ~9th Parameter	R	1	Checksum from "TR0 WF" to "TR8 WF"								-
10th Parameter	R	1	Checksum of "TR9 WF / backup 1"								-
11th Parameter	R	1	Checksum of "TR10 WF / backup 2"								-
12th Parameter	R	1	Checksum comparison result from "TR0 WF" to "TR7 WF"								-
13th Parameter	R	1	Checksum comparison result from "TR8" and "TR10 WF / backup 2"								-

Description

This command is to read checksum information from OTP.
1st to 11th Parameter : Checksum from "TR0 WF" to "TR10 WF / backup 2"
12th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
fault_TR7	fault_TR6	fault_TR5	fault_TR4	fault_TR3	fault_TR2	fault_TR1	fault_TR0

13th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	fault_TR10 / fault_backup2	fault_TR9 / fault_backup1	fault_TR9

definition of fault_TRx / fault_backup_x

Value	Function
0	Checksum comparison : Equal
1	Checksum comparison : Not Equal

Restriction

RF3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CAL_CHKSUM	W	0	1	1	1	1	0	0	1	1	F3H

Description

This command is used to Calculate Checksum of LUT Table

Restriction

9. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact withelectrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases,which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

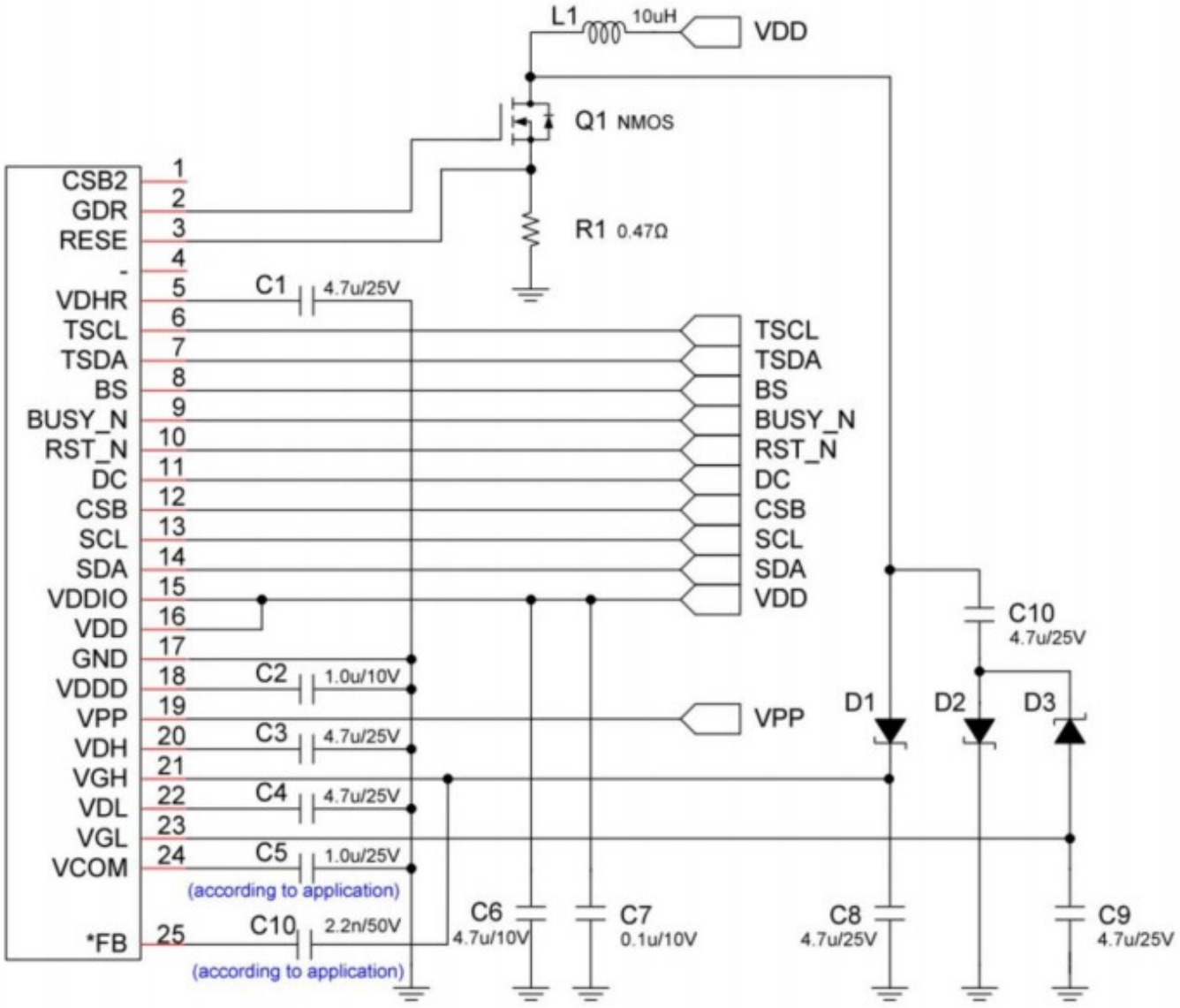
Observe general precautions that are common to handling delicate electronic components. Theglass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System(IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device.These are stress ratings only and operation of the device at these or at any other Conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

10. Reliability test

NO.	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70ºC，RH=40%，240 h Test in white pattern
3	High-Temperature Operation	T=40ºC，RH=35%，240 h
4	Low-Temperature Operation	0ºC，240h
5	High-Temperature, High-Humidity Operation	T=40ºC，RH=80%，240 h
6	High Temperature, High Humidity Storage	T=50ºC，RH=80%,240 h Test in white pattern
7	Temperature Cycle	1cycle:[-25°C 30min]→[+70°C 30min]: 50cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs, 40°C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display,no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display,including IC and FPC area)

11. Typical Application Circuit with SPI Interface



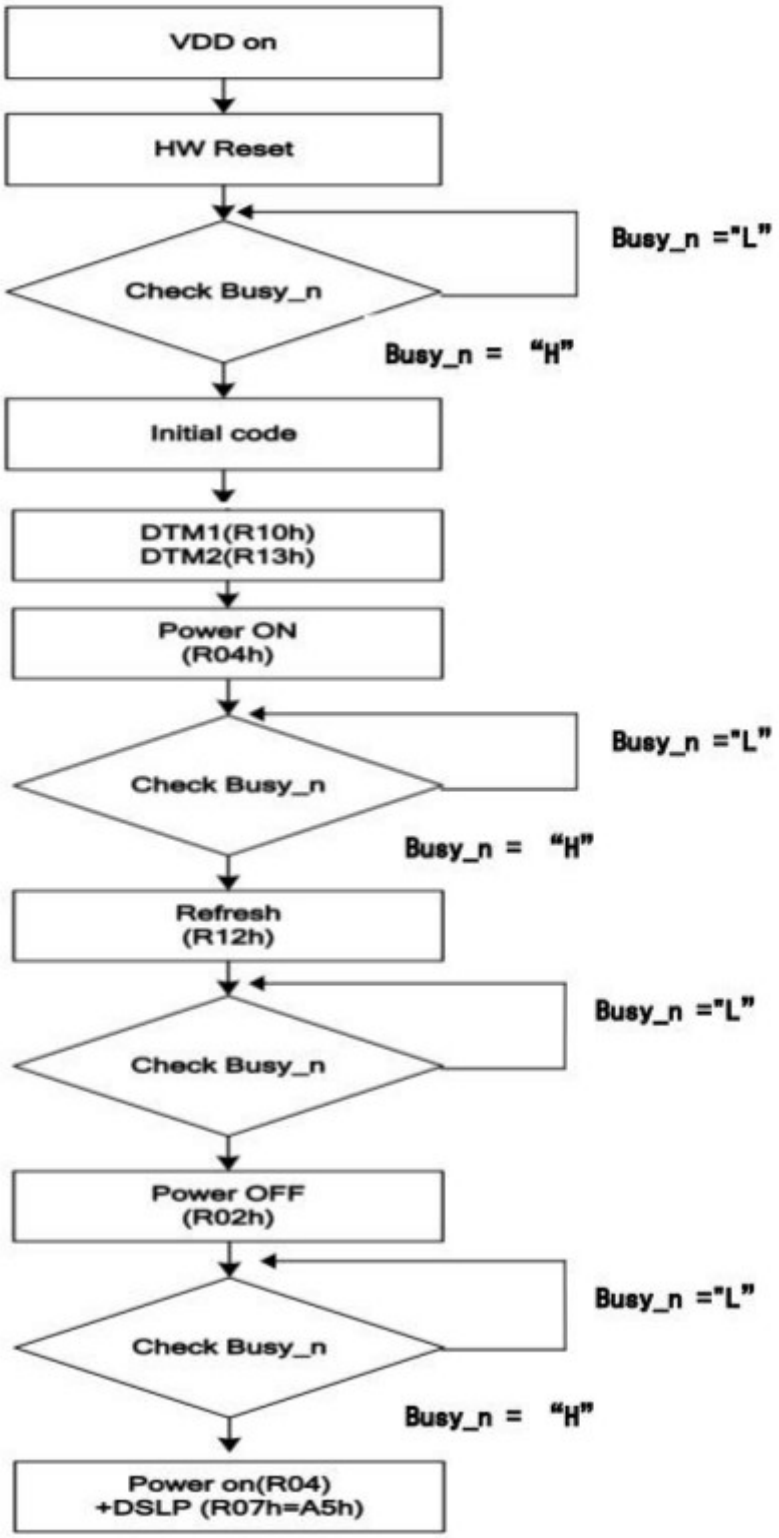
Note:

1. The capacitor value of VGH/VGL must be equal or more than the one of VDH/VDL/VDHR.

Recommended Device

1. Switch MOS NMOS: Vishay Si1308EDL (V_{DS} > 20V, I_D > 500mA, $V_{GS(th)}$ < 1.5V, C_{ISS} < 200pF, $R_{DS(on)}$ < 400mΩ)
2. Schottky Diode: OnSemi MBR0530 (V_R > 20V, I_F > 500mA, I_R < 1mA @ V_R=15V, T_A=100°C)
3. Inductance: Bourns SRN2010TA-1R5Y (DCR<0.5Ω, Isat>1.2A @ 25 °C)

12. Typical Operating Sequence



13. Inspection condition

13.1 Environment

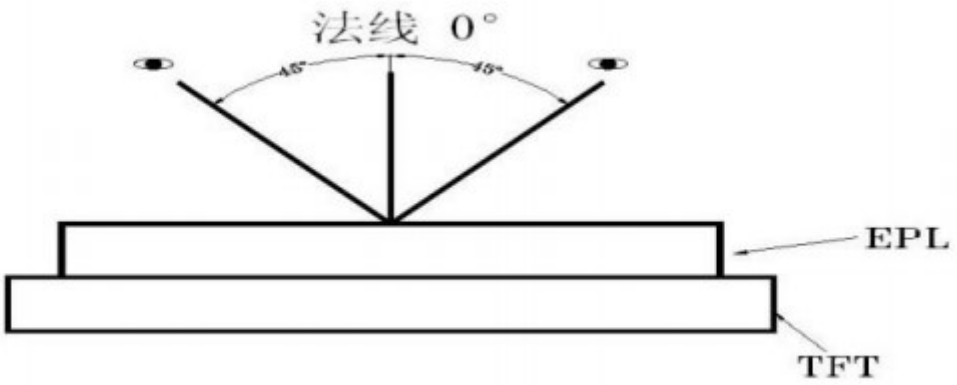
Temperature： 25±3 ℃

Humidity：55±10%RH

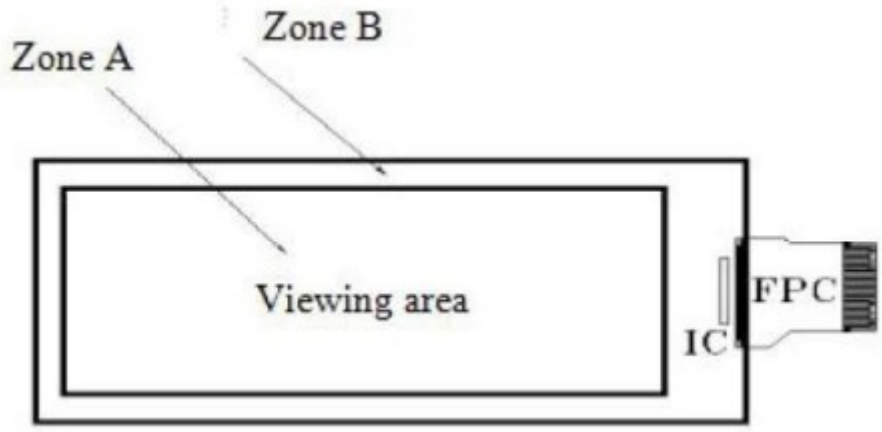
13.2 Illuminance

Brightness:1200～1500LUX; distance: 30CM; Angle: Relate 45°surround.

13.3 Inspect method

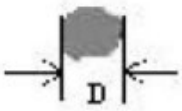
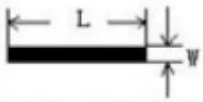


13.4 Display area

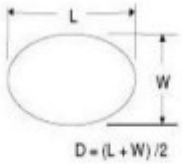
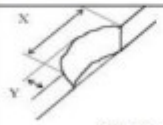
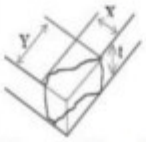
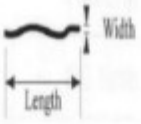


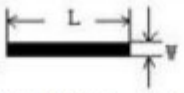
13.5 Inspection standard

13.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm。N≤3， 0.5mm＜D Not Allow	MI		
3	Black/White spots (No switch)	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

13.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm，N≤5 D＞0.5mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	D≤0.25mm, allow 0.25mm＜D≤0.4mm ,n≤4 allow D＞0.4mm is not allowed (n≤8 items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤5	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Zone B
14	Silicon glue	Thickness ≤ PS surface(With protect film): Full cover the IC; Shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 t≤1.5mm	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

14. Packaging

	常 备 库 存 Stock For Sale	长 期 供 货 Long Time supply	支持小量 NO MOQ	品 种 齐 全 In Full Range