



**SPECIFICATION  
FOR  
LCD MODULE**

**Customer** : \_\_\_\_\_  
**Product Model:** YH101MF4001  
**Sample code:** FX101-MM2QA01-A

Designed by	Checked by	Approved by

**Final Approval by Customer**

<input type="checkbox"/> <b>LCM Machinery OK</b> Checked By _____  <input type="checkbox"/> <b>LCM Display OK</b> Checked By _____	<input type="checkbox"/> <b>LCM OK</b>  <input type="checkbox"/> <b>NG , Problem survey:</b>  Approved By _____
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※The specification of "TBD" should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.





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## 1. GENERAL DESCRIPTION

### 1.1 DESCRIPTION

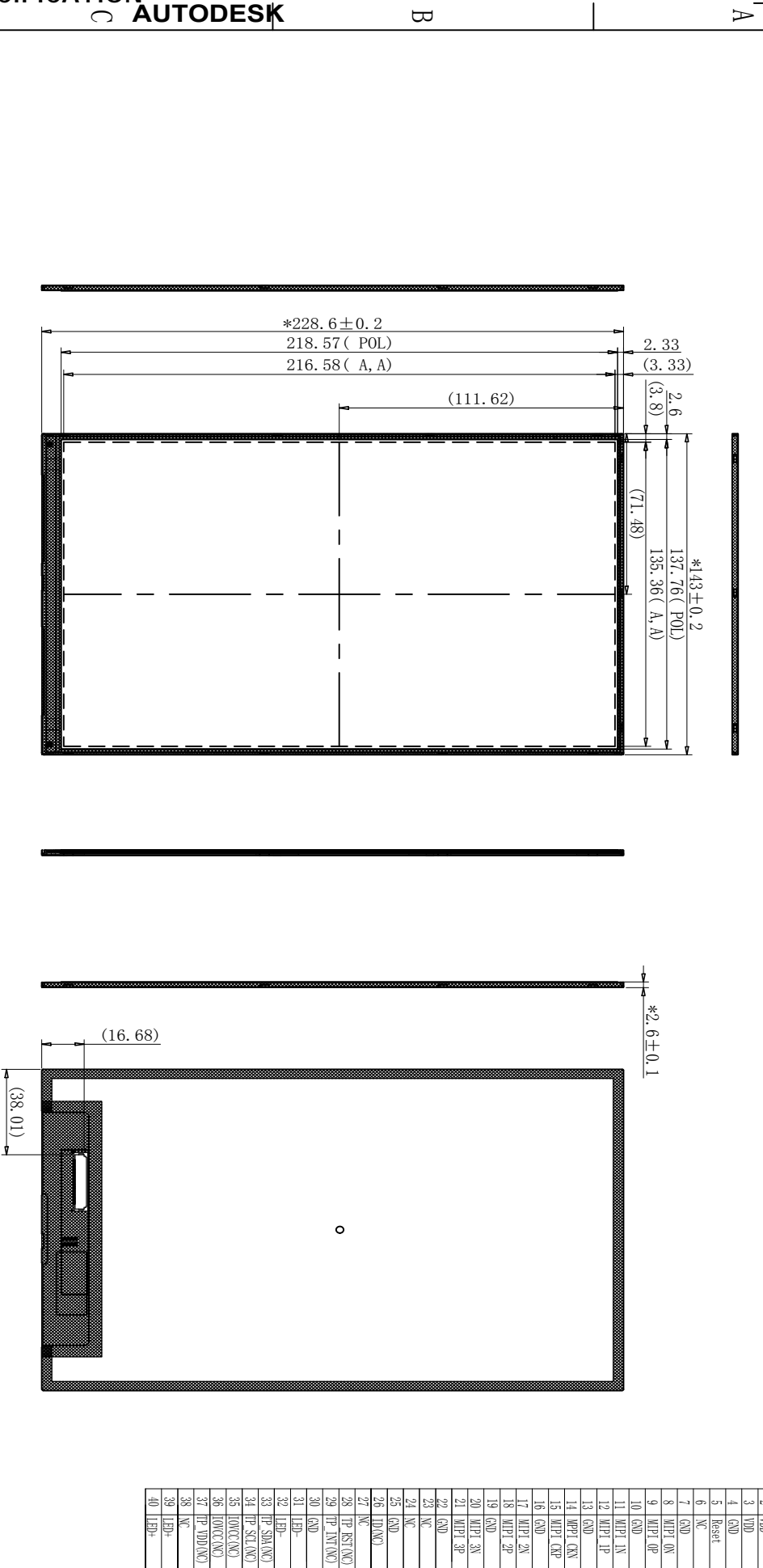
YH101MF4001 is a color active matrix thin film transistor (TFT) IPS liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, Driver IC ,FPC and Backlight.

### 1.2 FEATURES:

No.	Item	Specification	Unit
1	Panel Size	10.1”	inch
2	Number of Pixels	1200x3(RGB) x 1920	pixels
3	Active Area	135.360(W)x216.576(H)	mm
4	Pixel Pitch	0.1128 x 0.1128	mm
5	OutlineDimension	228.6(W) x 143(H) x2.6(D)	mm
6	Number of Colors	16.7M	-
7	Display Mode	Normally Black	-
8	ViewingDirection	IPS	
9	Pixel Arrangement	RGB vertical stripe	-
10	Luminance (cd/m <sup>2</sup> )	280(TYP.)	nit
11	Contrast Ratio	800(TYP)	
12	Surface Treatment	Anti-glare	-
13	Interface	MIPI	-
14	Backlight	White LED	-
15	Operation Temperature	-10-50	°C
16	Storage Temperature	-20-60	°C
17	Weight	TPD	g

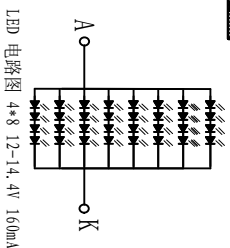


1	NC
2	VDD
3	VDD
4	GND
5	Reset
6	NC
7	GND
8	MEP1_0N
9	MEP1_0P
10	GND
11	MEP1_1N
12	MEP1_1P
13	GND
14	MEP1_0N
15	MEP1_0P
16	GND
17	MEP1_2N
18	MEP1_2P
19	GND
20	MEP1_3N
21	MEP1_3P
22	GND
23	NC
24	NC
25	GND
26	DP(NC)
27	NC
28	TP_RST(NC)
29	PP_INT(NC)
30	GND
31	LED+
32	LED-
33	PP_SDA(NC)
34	PP_SCL(NC)
35	IOWC(NC)
36	IOWC(NC)
37	PP_VDD(NC)
38	NC
39	LED+
40	LED-



## 2. MECHANICAL SPECIFICATION

- NOTES:
1. DISPLAY TYPE: 10.1";
  2. VIEWING DIRECTION: IPS ;
  3. LCM Chromaticity(White): X 0.31+/-0.03; Y 0.32+/-0.03;
  4. OPERATING TEMP: -10° C TO 50° C;
  5. STORAGE TEMP: -20° C TO 60° C;
  6. BACK LIGHT: 32 CHIP WHITE LED;
  7. LUMINANCE (9 AVG): 260 cd/m² (MIN), 280 cd/m² (TYP) ;
  8. Uniformity (%): 70% (MIN) 75 (TYP) ;
  9. Dimensions with mark "\*" are important, with mark "(") are referenced;
  10. General Tolerance: ±0.2
  11. Requirements Environmental Protection: RoHS;



REV	DATE	DESCRIPTION	REVISION	TYPE	MODEL NO.	EDITION	APPROVED
修改	日期	修改内容	修改者	类型	模组号	版本号	承认
				LCM	YH101MF4001	A0	
					YH101MF4001	1/1	
					YH101MF4001	20_09_07	



### 3. PIN DESCRIPTION

<b>PIN NO.</b>	<b>Symbol</b>	<b>Description</b>
1	NC	No connection
2	VDD	Power Voltage for digital circuit 3.3V
3	VDD	Power Voltage for digital circuit 3.3V
4	GND	Ground
5	Reset	Global reset pin 3.3V
6	NC	No connection
7	GND	Ground
8	MIPI_0N	-MIPI differential data input
9	MIPI_0P	+MIPI differential data input
10	GND	Ground
11	MIPI_1N	-MIPI differential data input
12	MIPI_1P	+MIPI differential data input
13	GND	Ground
14	MIPI_CKN	-MIPI differential clock input
15	MIPI_CKP	+MIPI differential clock input
16	GND	Ground
17	MIPI_2N	-MIPI differential data input
18	MIPI_2P	+MIPI differential data input
19	GND	Ground
20	MIPI_3N	-MIPI differential data input
21	MIPI_3P	+MIPI differential data input
22	GND	Ground
23	NC	No connection
24	NC	No connection
25	GND	Ground
26	NC	No connection
27	PWMO	PWM control signal for LED driver(CABC)
28	NC	No connection
29	NC	No connection
30	GND	Ground



31	LED-	LED Cathode
32	LED-	LED Cathode
33	NC	No connection
34	NC	No connection
35	NC	No connection
36	NC	No connection
37	NC	No connection
38	NC	No connection
39	LED+	LED Anode
40	LED+	LED Anode

#### 4. Absolute Max. Rating

Item	Symbol	Values		Unit
		Min.	Max.	
Power Voltage	VCC	-0.3	+5.0	V
Backlight forward current	I <sub>LED</sub>	0	25	mA(For each LED)
Input Signal Voltage	V <sub>I</sub>	-0.3	VCC	V
Operation Temperature	T <sub>OP</sub>	-10	50	°C
Storage Temperature	T <sub>ST</sub>	-20	60	°C

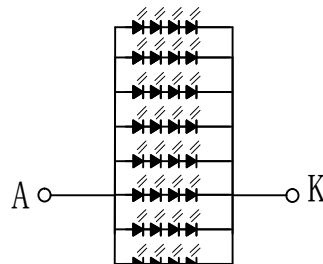
#### 4.1 Typical Operation Conditions

Item	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	3.0	3.3	3.6	V
Current Consumption	I <sub>VCC</sub>	-	--	TBD	mA
	I <sub>LED</sub>		160		mA

#### 4.2 LED Back Light Specification (21 White Chips)

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	V <sub>f</sub>	I <sub>f</sub> =160mA	11.2	-	13.4	V
Uniformity (with L/G)	Δ B <sub>p</sub>	I <sub>f</sub> =160mA	75	80	-	%
Luminance for LCM	/	I <sub>f</sub> =160mA	260	280	-	cd/m <sup>2</sup>

LED circuit:

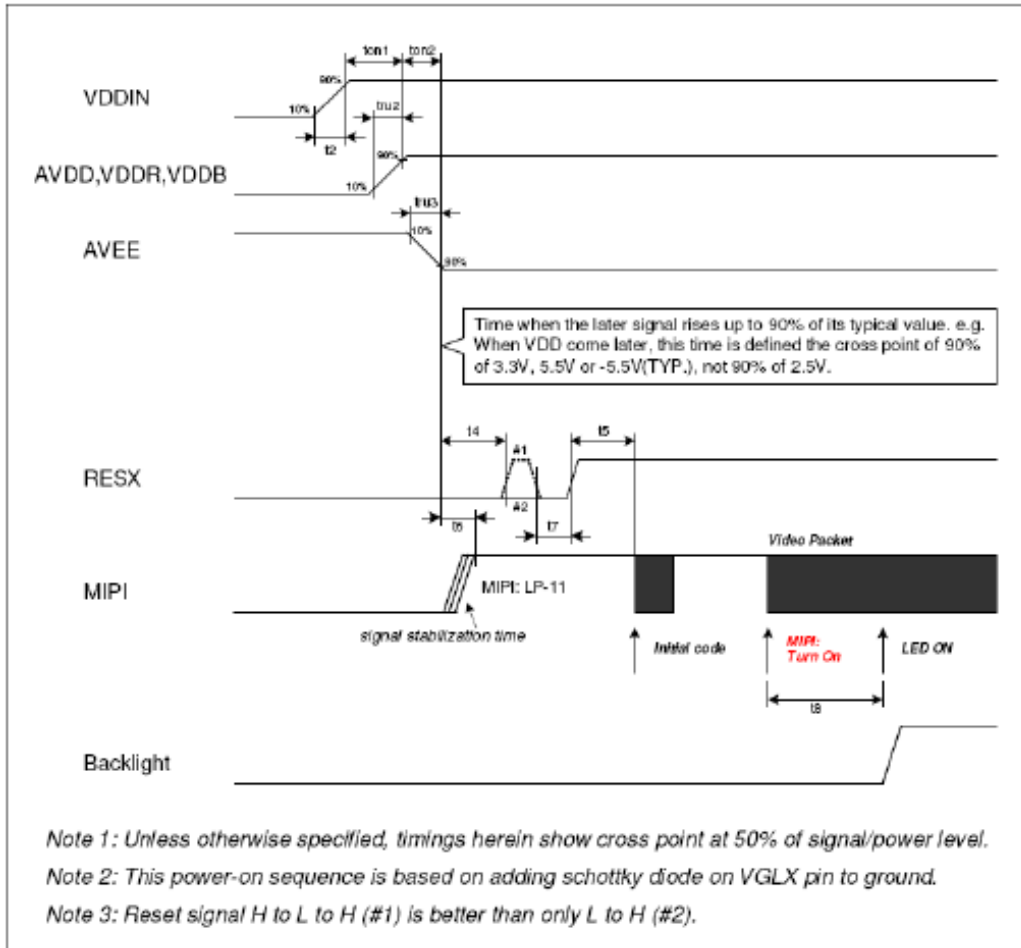


LED 电路图 4\*8



## 5. Signal timing diagram Power Sequence

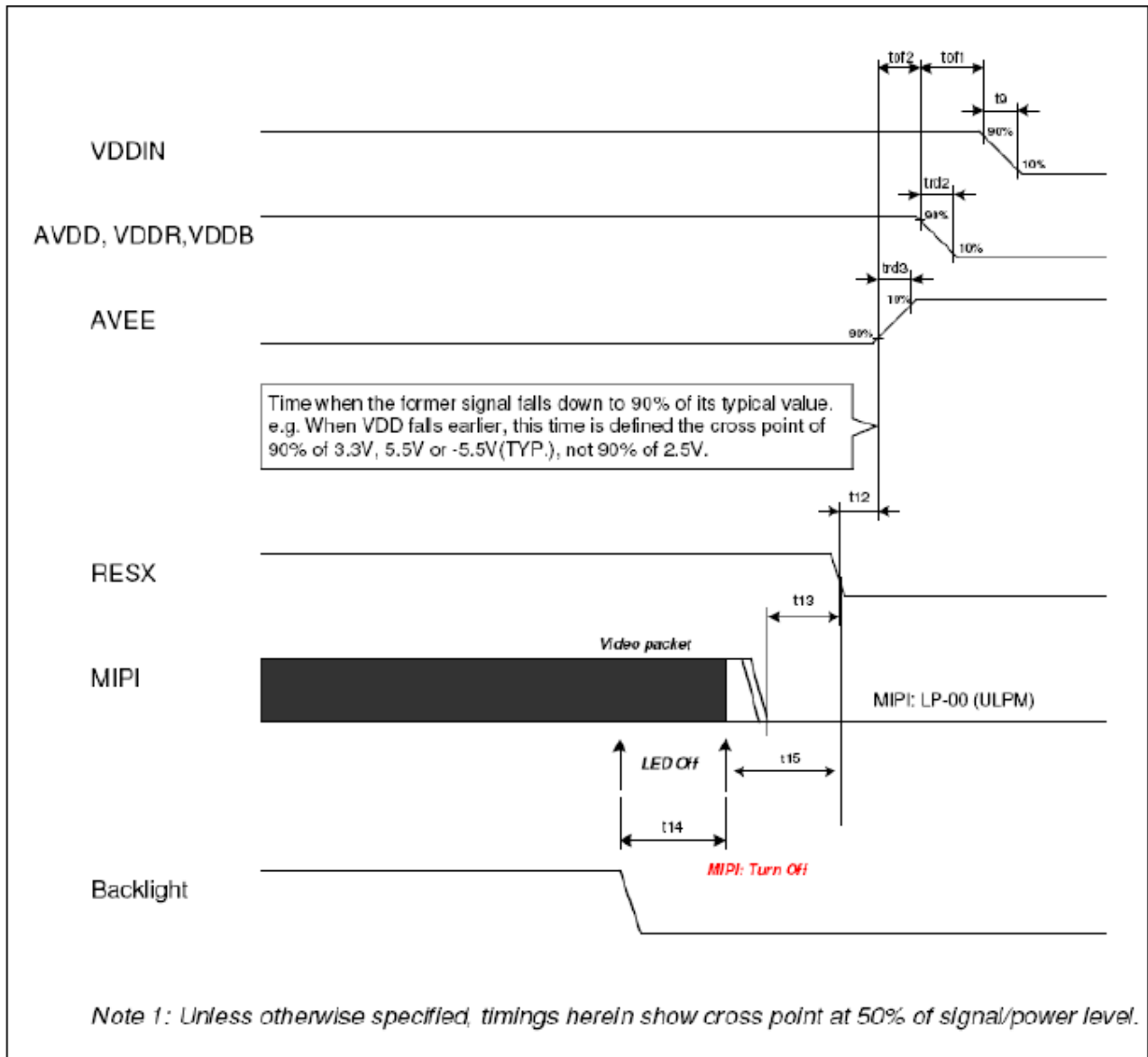
### 5.1 Power on



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1		No limit		ms	
ton2		0(Note)		ms	
ton3		No limit	-	ms	
ton4		No limit	-	ms	
t2			150	μs	
tru1			150	μs	
tru2			150	μs	
tru3			150	μs	
tru4			150	μs	
t4	40	-	-	ms	
t5	120			ms	
t6	0			ms	
t7	10			μs	
t8	8			VS	Keep data more than 8 frames (VS)



## 5.2 Power off





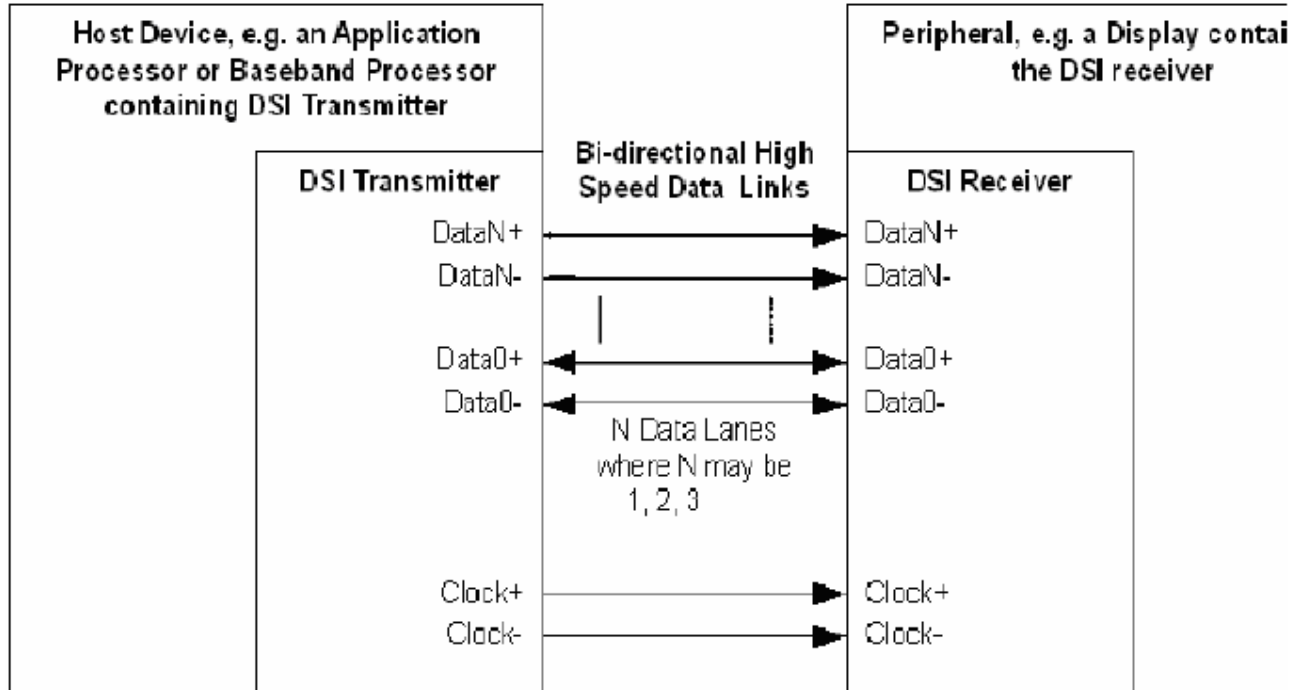
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150			μs	
tof1		No limit		ms	
tof2		0(Note)	-	ms	
tof3		No limit	-	ms	
tof4		No limit		ms	
trd1	150			μs	
trd2	150			μs	
trd3	150			μs	
trd4	150			μs	
t12	0		-	ms	
t13	0			ms	
T14	0			ms	
T15	10			ms	

### 5.3 MIPI Timing characteristics

#### 5.4 MIPI Lane Configuration

	MCU (Master)	Display Module (Slave)
Clock Lane+/-	Unidirectional Lane <ul style="list-style-type: none"> <li>■ Clock Only</li> <li>■ Escape Mode(ULPS Only)</li> </ul>	
Data Lane0+/-	Bi-directional Lane <ul style="list-style-type: none"> <li>■ Forward High-Speed</li> <li>■ Bi-directional Escape Mode</li> <li>■ Bi-directional LPDT</li> </ul>	
Data Lane1+/-	Unidirectional <ul style="list-style-type: none"> <li>■ Forward High speed</li> </ul>	
Data Lane2+/-	Unidirectional <ul style="list-style-type: none"> <li>■ Forward High speed</li> </ul>	
Data Lane3+/-	Unidirectional <ul style="list-style-type: none"> <li>■ Forward High speed</li> </ul>	

The connection between host device and display module is as reference.



## 6. MIPI AC Electrical characteristics

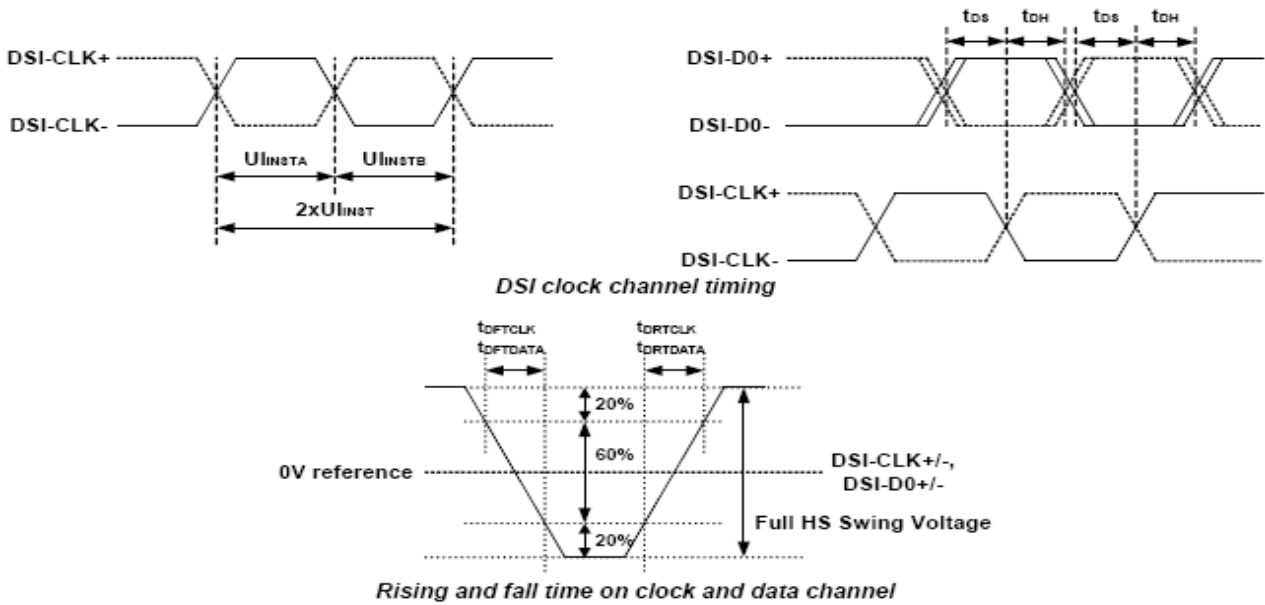
### 6.1 High Speed Transmission

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2 \times UI_{INST}$	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	$UI_{INSTA}$ $UI_{INSTB}$	UI instantaneous halves ( $UI = UI_{INSTA} = UI_{INSTB}$ )	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	$t_{DS}$	Data to clock setup time	$0.15 \times UI$	-	-	ps	
DSI-Dn+/-	$t_{DH}$	Data to clock hold time	$0.15 \times UI$	-	-	ps	
DSI-CLK+/-	$t_{DRTCLK}$	Differential rise time for clock	150	-	$0.3 \times UI$	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	$0.3 \times UI$	ps	
DSI-CLK+/-	$t_{DFTCLK}$	Differential fall time for clock	150	-	$0.3 \times UI$	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	$0.3 \times UI$	ps	

Note 1) Dn = D0, D1, D2 and D3.

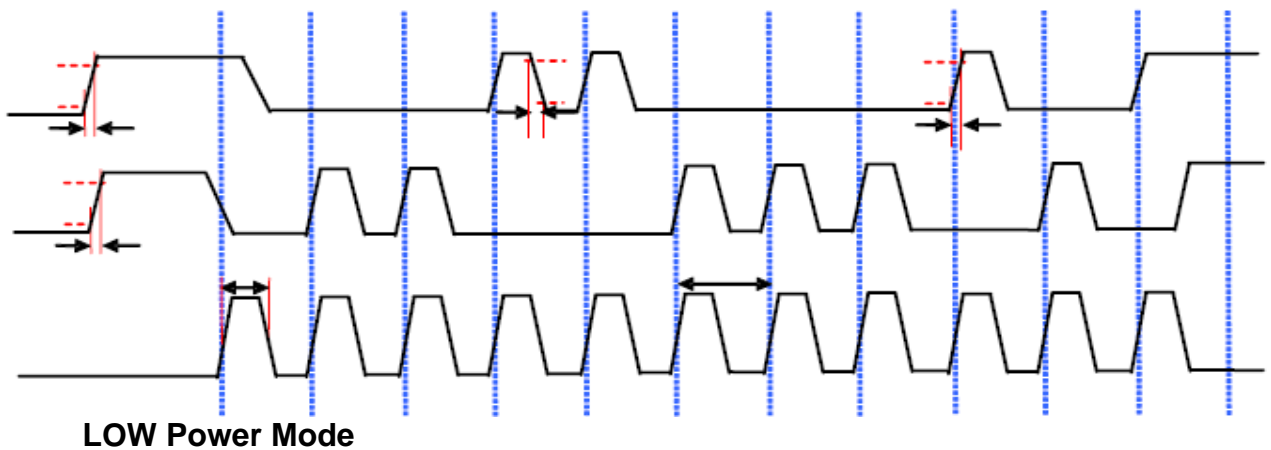
Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format



## 6.2 LP Transmission

Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	$F_{DSICLK\_LP}$			10	MHz	
DSI CLK Cycle Time(LP)	$t_{CLKC\_LP}$	100			ns	
DSI Data Transfer Rate(LP)	$t_{DSIR\_LP}$			10	Mbps	
15%-85% rise time and fall time	$T_{RLP} / T_{FLP}$	-	-	35	ns	
30%-85% rise time(from HS to LP)	$T_{REOT}$	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP-PULSE-TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP-PRE-TX}$	100	130	-	ns	





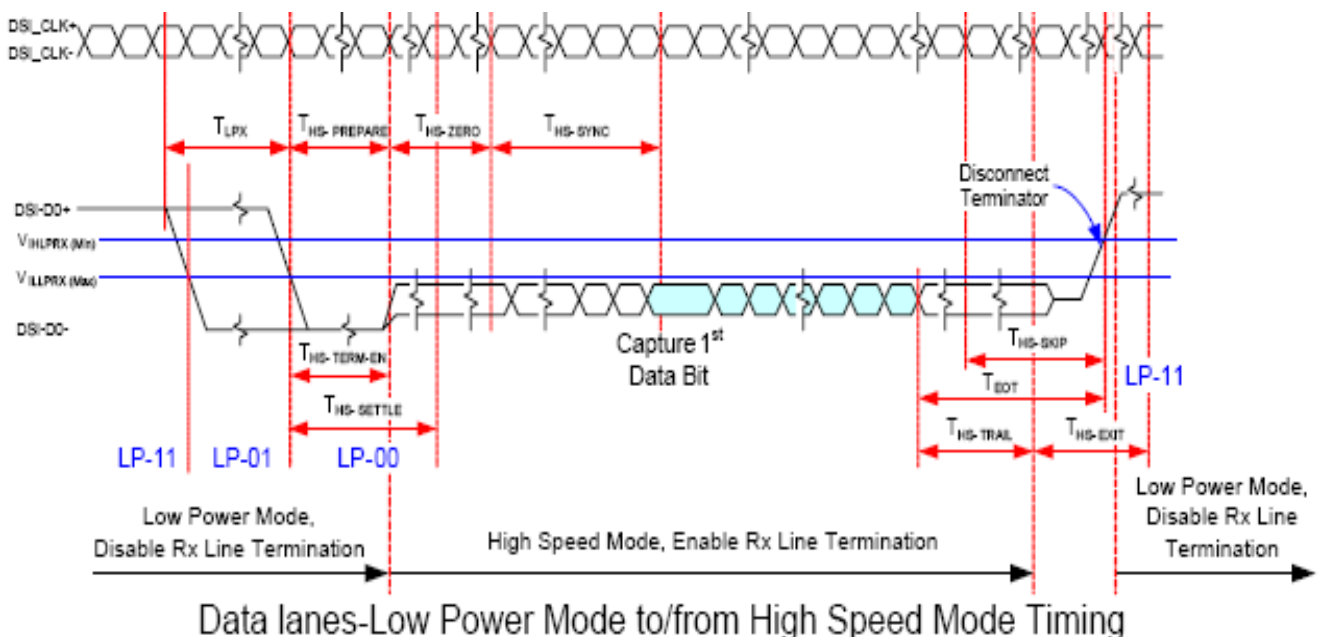


### 6.3 DSI Bursts

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T <sub>LFX</sub>	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	T <sub>HS-PREPARE</sub>	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	T <sub>HS-TERM-EN</sub>	Time to enable data receiver line termination measured from when Dn crosses V <sub>ILMAX</sub>	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	T <sub>HS-SKIP</sub>	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	T <sub>HS-EXIT</sub>	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	T <sub>HS-TRAIL</sub>	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	T <sub>CLK-POS</sub>	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	T <sub>CLK-TRAIL</sub>	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	T <sub>HS-EXIT</sub>	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	T <sub>CLK-PREPARE</sub>	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	T <sub>CLK-TERM-EN</sub>	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input

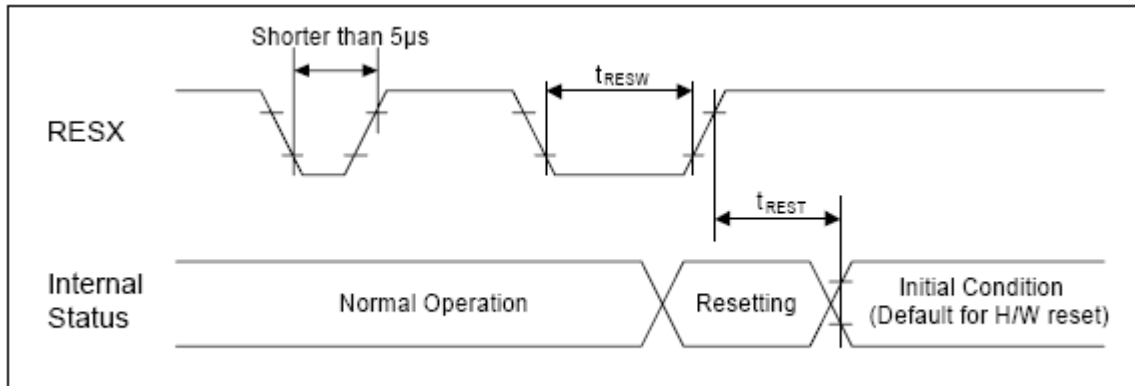
Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as T<sub>HS-EXIT</sub> from each other in continuous clock mode. In discontinuous mode, the break is longer which account T<sub>CLK-POS</sub>, T<sub>CLK-TRAIL</sub> and T<sub>HS-EXIT</sub>, before activity in clock and data lanes again.





## 6.4 Reset Input Timing



Reset input timing

( $V_{DD1}=1.7\sim 1.9V$ ,  $V_{CI}=3.0$  to  $3.6V$ ,  $GND=0V$ ,  $T_a = -30$  to  $70^\circ C$ )

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	$t_{RESW}$	Reset "L" pulse width (Note 1)	10	-	-	$\mu s$	
	$t_{REST}$	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

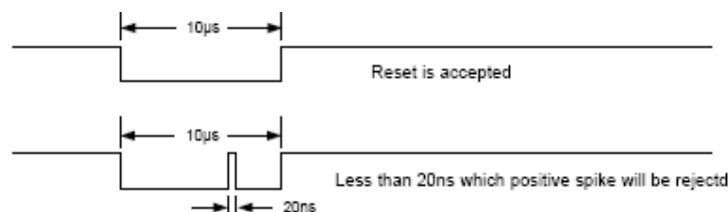
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than $5\mu s$	Reset Rejected
Longer than $10\mu s$	Reset
Between $5\mu s$ and $10\mu s$	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In-mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time ( $t_{REST}$ ) within 5ms after a rising edge of RESX.

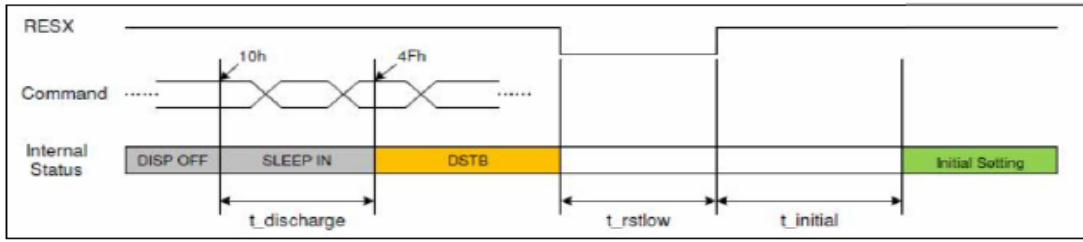
Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec



### 6.5 Deep Standby Mode Timing



(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t <sub>discharge</sub>	Sleep in into DSTB delay time	-	-	100	ms	
	t <sub>rstlow</sub>	Reset low pulse	3	-	-	ms	
	t <sub>initial</sub>	Reset high to initial setting delay time	-	-	120	ms	

Note 1) t<sub>discharge</sub> suggested delay time over 100ms.

Note 2) t<sub>initial</sub> suggested delay time over 120ms..

### 6.6 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V <sub>CMCLK</sub> V <sub>CMDATA</sub>	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	V <sub>CMRCLKL</sub> V <sub>CMRDATAL</sub>	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	V <sub>CMRCLKM</sub> V <sub>CMRDATAM</sub>	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V <sub>THCLK</sub> V <sub>THDATA</sub>	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V <sub>THCLK</sub> V <sub>THDATA</sub>	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V <sub>ILHS</sub>	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V <sub>IHHS</sub>	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R <sub>TERM</sub>	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	V <sub>TERM-EN</sub>	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C <sub>TERM</sub>	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

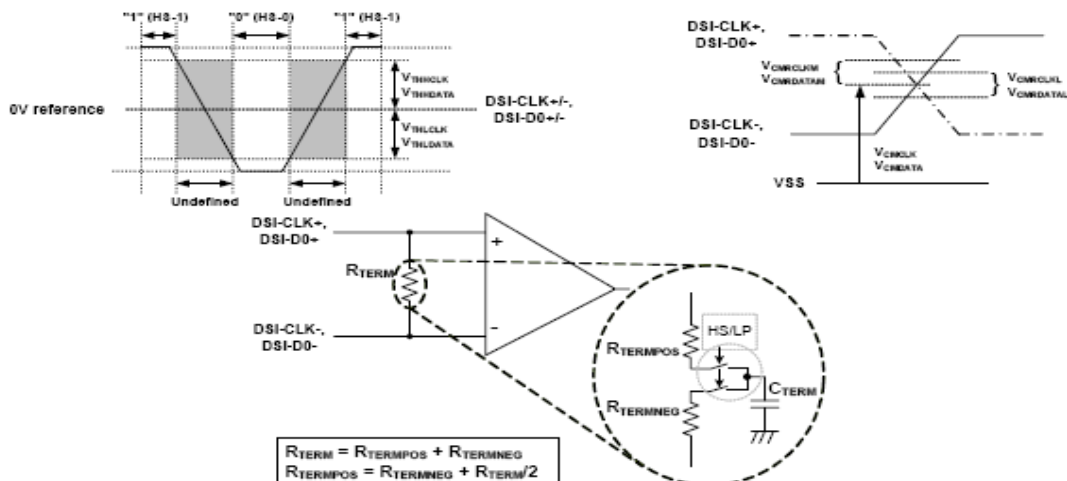
Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 °C (to +85 °C no damage).

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

Note 3) Without VCMRCLKM / VCMRDATAM .

Note 4) Without 50mV (-50mV to 50mV) ground difference.

Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage



## 7. Optical Specifications

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark		
Viewing Angle range	Horizontal	$\Theta_3$	CR > 10	80	89	-	Deg.	WV-Pol Note 1		
		$\Theta_9$		80	89	-	Deg.			
	Vertical	$\Theta_{12}$		80	89	-	Deg.			
		$\Theta_6$		80	89	-	Deg.			
Luminance Contrast ratio		CR		700	800	-		-		
Cell Transmittance		Tr		-	4.6%	-	%			
White Chromaticity		$x_w$	$\Theta = 0^\circ$	0.27		0.33		Note 4 CF Glass		
		$y_w$		0.29		0.35				
Reproduction of color (C light)	Red	$R_x$		-	0.614	-				
		$R_y$		-	0.363	-				
	Green	$G_x$		-	0.528	-				
		$G_y$		-	0.343	-				
Blue	$B_x$	-		0.108	-					
	$B_y$	-		0.271	-					
Color Gamut (C light)					-	55	-		%	NTSC
Response Time (Rising + Falling)		$T_{RT}$		Ta= 25° C $\Theta = 0^\circ$	-	30	40		ms	Note 5



Note 1: Definition of viewing angle range

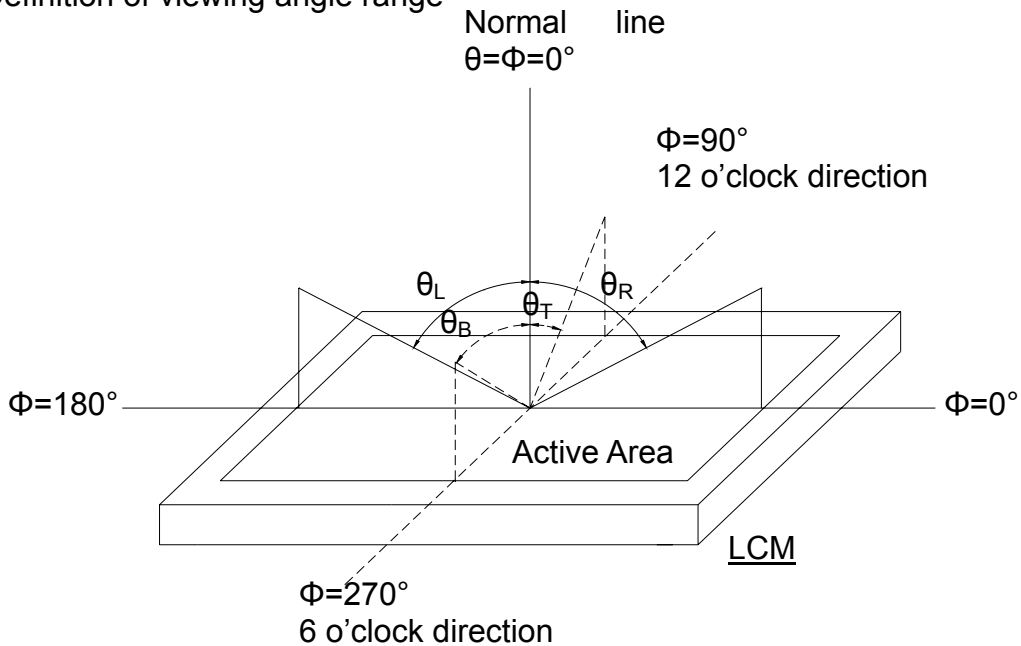


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm ,Response time is measured by Photo detector TOPCON BM-5A, other items are measured by BM-7A/Field of view: 1° /Height: 500mm.)

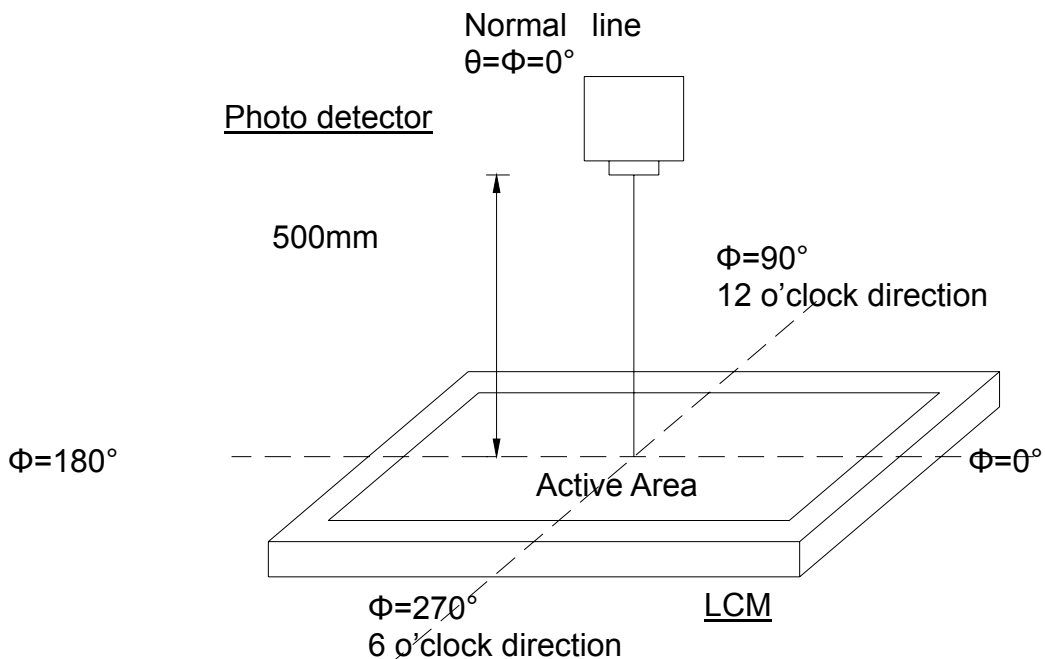


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time ( $T_{ON}$ ) is the time between photo detector output intensity changed from 90% to 10%. And fall time ( $T_{OFF}$ ) is the time between photo



detector output intensity changed from 10% to 90%.

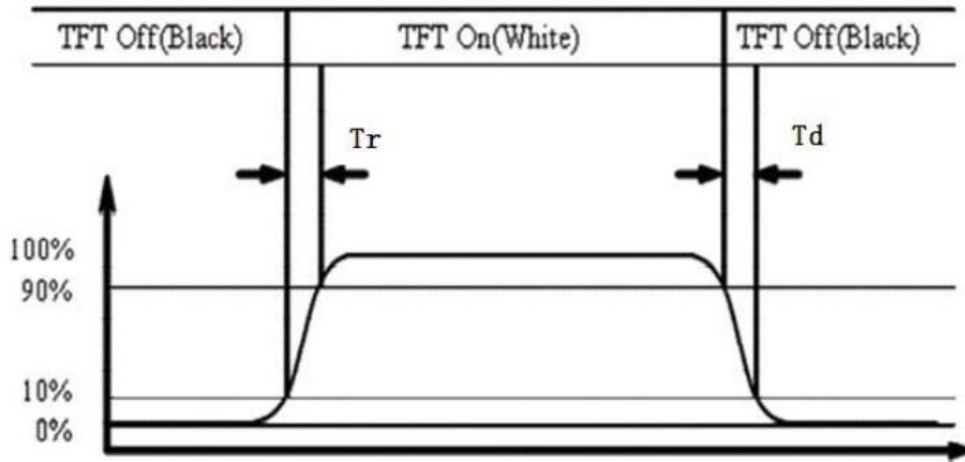


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is  $I_{LED}=160\text{mA}$ .

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4 ).Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (Yu)} = \frac{B_{min}}{B_{max}}$$

L-----Active area length      W----- Active area width

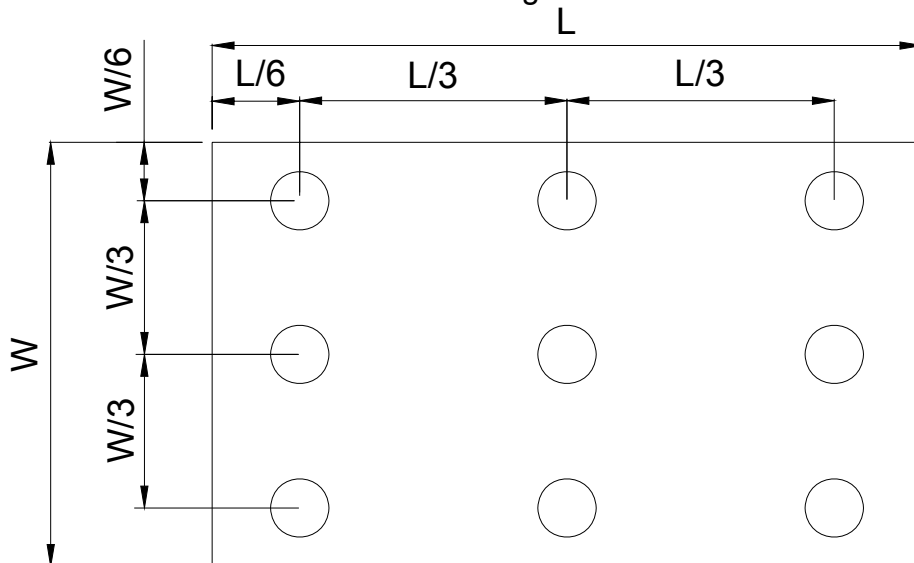


Fig. 4-4 Definition of measuring points

$B_{max}$ : The measured maximum luminance of all measurement position.

$B_{min}$ : The measured minimum luminance of all measurement position.